

IDENTIFICATION

PRODUCT CODE: AH-?????-DD
DIAGNOSTIC CODE: DCKAD
PRODUCT NAME: DFKAD80 PDP10 KL10 BASIC INSTRUCTION
DIAGNOSTIC #4
VERSION: 0.2
DATE RELEASED: SEPT 1984
MAINTAINED BY: DIAGNOSTIC ENGINEERING
AUTHOR: JOHN A. KIRCHOFF

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1.C ABSTRACT

THIS DECSYSTEM KL10 BASIC INSTRUCTION DIAGNOSTIC IS THE FOURTH IN A SERIES OF DECSYSTEM KL10 PROCESSOR DIAGNOSTICS. THE DIAGNOSTIC TESTS INDEXED ADDRESSING, INDIRECT ADDRESSING, INDEXED-INDIRECT ADDRESSING AND ARITHMETIC FLAGS TESTS. THE DIAGNOSTIC ALSO PERFORMS TESTS OF THE FOLLOWING INSTRUCTIONS: EXCH, MOVEM, JFCL, ADDI, CAI, JRST, JSP, AOBJN, AOBJP, AOS, SOS, JUMPL, JUMPE, JUMPB, JUMPG, AOJ, SOJ, ADDM, HRREM, MOVSM, XORM, ADDB, HLLOS, MOVSS, HRLM, HRRS, HRRZM, SETZB, SETAB, XCT.

THE DIAGNOSTIC TESTS THE BASIC FUNCTIONALITY OF THE R AND MICROPROCESSOR.

2.0 REQUIREMENTS

2.1 EQUIPMENT

A KL10 WITH A MINIMUM OF 32K OF MEMORY.

CONSOLE TELETYPE.

2.2 STORAGE

THE PROGRAM RUNS WITHIN 128K OF MEMORY.

2.3 PRELIMINARY PROGRAMS

CONSOLE FUNCTIONS WORKING PROPERLY.
PREVIOUS PROCESSOR DIAGNOSTICS.

3.0 PROGRAM PROCEDURES

3.1 LOADING PROCEDURE

LOAD VIA APPROPRIATE LOADING PROCEDURES.

3.2 STARTING PROCEDURE

STAND-ALONE STARTING ADDRESS IS 40000.

IF THE DIAGNOSTIC FAILS TO START CORRECTLY TRY STARTING AT THE FIRST TEST INSTEAD OF AT THE BEGINNING OF THE CONTROL SEQUENCE. (SEE LISTING).

3.3 OPERATING PROCEDURE

ONCE STARTED THE PROGRAM WILL CYCLE CONTINUALLY UNTIL STOPPED OR AN ERROR OCCURS.

4.0 ERRORS

ERRORS ARE IN THE FORM OF HALT INSTRUCTIONS. THE LISTING SHOULD BE CONSULTED TO DETERMINE THE CAUSE OF THE ERROR. A NO OPERATION (JUMP) INSTRUCTION FOLLOWS EACH HALT. THIS MAY BE USEFUL IN CONSTRUCTING A SCOPE LOOP TO CYCLE ON THE FAILING INSTRUCTION.

5.0 ITERATION COUNTER

THE ITERATION COUNT OF THE PROGRAM CAN BE DETERMINED BY EXAMINING LOCATION 'PASCNT'.

6.0 CYCLE TIME

THE CYCLE TIME OF THE PROGRAM IS IN THE MILLISECOND RANGE AND IS THEREFORE SUITABLE FOR TAKING MARGINS, VIBRATION TESTS, ETC.

7.0 OPERATIONAL VARIATIONS

A. DIAGNOSTIC MONITOR

THE PROGRAM IS USABLE WITH THE DIAGNOSTIC MONITOR TO PROVIDE RELIABILITY TESTS, ACCEPTANCE TESTS, AND / OR TO PROVIDE A QUICK METHOD OF ISOLATION OF A FAULT TO A PARTICULAR AREA OF THE PROCESSOR. CERTAIN PROCEDURES ARE USED WHEN THE PROGRAM IS USED IN THIS MANNER. THEY ARE:

1. THE DIAGNOSTIC MONITOR TRANSFERS CONTROL TO THE PROGRAM AND STARTS IT AT LOCATION 40002.
2. MONCTL - LOCATION 40064 IS USED AS THE DIAGNOSTIC MONITOR CONTROL FLAG WORD.

B. USER MODE

THE PROGRAM WILL OPERATE IN USER MODE AND AS SUCH PROVIDES ASSURANCE THAT THE PROCESSOR IS PERFORMING ALL FUNCTIONS CORRECTLY. USER MODE STARTING ADDRESS IS 40000.

C. SYSTEM EXERCISER

STARTING ADDRESS IS 40003. NO DATA SWITCHES ARE USED BY THIS PROGRAM.

8.0 MISCELLANEOUS

NONE

9.0 LISTING

HISTORY FILE FOR DCKAD

SEQ 0006

CODE: MAINDEC-10-DCKAD
TITLE: DECSYSTEM KC10 BASIC INSTRUCTION DIAGNOSTIC (4)
VERSION: 0.2
DATE: August 1982
REASCN: Reassembled for changes to SPCCPU.KCM

CODE: MAINDEC-10-DCKAD
TITLE: DECSYSTEM KC10 BASIC INSTRUCTION DIAGNOSTIC (4)
VERSION: 0.1
DATE: March 1982
REASON: ORIGINAL RELEASE OF THIS PROGRAM FOR KC10.
NOTE: THIS PROGRAM WAS ADAPTED FROM 'DSKAD' -
AN ANALOGOUS PROGRAM FOR THE DECSYSTEM
2020 KS-10.

```
1      ;DFKAD
2
3      000000      MCNVER==0
4      000002      DECVER==2
5
6      XLIST
7      LIST
8      LALL
9
10     NAME      \MCNVER,\DECVER^
11
12     TITLE     DFKAD PDP10 KL10 BASIC INSTRUCTION DIAGNOSTIC (4) 0,2
13
14
15     ;BYTE, BLOCK TRANSFER, JFFO AND OTHER BASIC MISCELLANEOUS INSTRUCTIONS
16
17     ;COPYRIGHT 1984
18     ;DIGITAL EQUIPMENT CORPORATION
19     ;MARLBORO, MASS. 01752
20
21     ;J. Kirchoff
22
23     000137      LOC      137
24     000137      000000      000002      MCNVER,,DECVER
25
26     NOSYM
```

```

27      SUBTTL  DIAGNOSTIC PARAMETERS
28
29      ;Parameter definitions
30      000040  DEBUG=40
31      000001  EXCASB==1
32      000001  USRASB==1
33      000001  KI10=1
34      000001  KL10=1
35      000001  KL10PO=1
36      000001  PGMEND==1
37      000001  ERDIAG=1
38      000000  MEMMAP==0
39
40
41      ;SPECIAL FEATURE DEFINATIONS
42
43      030000  SADR1=BEGIN
44      030000  SADR2=BEGIN
45      030000  SADR3=BEGIN
46      030000  SADR4=BEGIN
47      254000  SADR5=JRST BEGIN
48      254000  SADR6=JRST BEGIN
49      254000  SADR7=JRST BEGIN
50      254000  SADR8=JRST BEGIN
51      254000  SADR9=JRST BEGIN
52      254000  SADR10=JRST BEGIN
53      254000  SADR11=JRST BEGIN
54
55      ;SPECIAL FEATURE PARAMETERS
56
57      000000  PAREA0=0
58      000000  PAREA1=0
59      000000  PAREA2=0
60      444653  414400  PAREA3=SIXBIT/DFKAD/
61      546064  000000  PAREA4=SIXBIT/LPT/
62      000000  PAREA5=0
63      000000  PAREA6=0
64      001000  ITERAT==1000
65
66      ;Macros
67
68      ; Stop - used for scope loop, if instruction fails, change (jumpa .+1)
69      ;          To a (jumpa .-x) to cycle on failing instruction
70
71      DEFINE  STOP      (A)<
72      HALT      .+1      ;Test failed if program halts here
73      JUMPA     .+1      ;To loop change this instruction>
74
75      ; Sflag - used to clear all flags then to set selected flag
76
77      DEFINE  SFLAG     (A)<
78      MOVSI     1,A
79      JFCL      17, .+1      ;Reset all flags
80      JRST      2, .+1(1)    ;Set a flag>
81

```



```
117 SUE:TTL *PARAM* PROGRAM/SUBROUTINE PARAMETERS, SEPT 18,1979
118
119 ; *****
120 ; *SPECIAL SUBPROGRAM LINKAGES
121 ; *****
122
123 027772 FSELNK= 27772 ;FILE SELECT LINK
124 027773 FRDLNK= 27773 ;FILE READ LINK
125 027774 LDLNK= 27774 ;LOAD LINKAGE ADDRESS
126 027775 DDTLNK= 27775 ;DDT LINKAGE ADDRESS
127 027776 MODLNK= 27776 ;OPERATIONAL MODE CHECK LINKAGE ADDRESS
128 027777 SUBLNK= 27777 ;SUBROUTINE LINKAGE ADDRESS
129
130 ; *****
131 ; *SPECIAL SUBROUTINE FATAL HALTS
132 ; *USED TO REPORT ERRORS THAT CAUSE THE SUBROUTINES TO BE UNUSABLE
133 ; *****
134
135 ;ADDRESS TAG REASON
136 ;-----
137
138 ; 1010 NOEXEC ;PROGRAM NOT CODED FOR EXEC MODE OPERATION
139 ; 1011 PLERR ;FATAL PUSH LIST POINTER ERROR
140 ; 1012 PLERR1 ;INITIAL PUSH LIST POINTER ERROR
141 ; 1013 MUOERR ;MUUO WITH LUUO HANDLER WIPED OUT
142 ; 1014 DTEBER ;DTE20 INTERRUPT WITHOUT DOORBELL
143 ; 1015 DTECER ;DTE20 CLOCK INTERRUPT WITHOUT FLAG SET
144 ; 1016 CPIERR ;CPU INITIALIZATION ERROR
145 ; 1017 EOPERR ;END OF PROGRAM ERROR
146 ; 1020 LUOERR ;INTERRUPT WITH LUUO HANDLER WIPED OUT
147
148 ; *****
```



```

149      ; *****
150      ; OPERATOR DEFINITIONS (NON-UUO'S)
151      ; *****
152
153      260740 000000 OPDEF GO [PUSHJ P,] ;SUBROUTINE CALL
154      263740 000000 OPDEF RTN [POPJ P,] ;SUBROUTINE RETURN
155      261740 000000 OPDEF PUT [PUSH P,] ;PUT DATA ON PUSH LIST
156      262740 000000 OPDEF GET [POP P,] ;GET DATA FROM PUSH LIST
157      254000 000000 OPDEF PJRST [JRST ] ;JRST TO ROUTINE THAT RTN'S
158      254200 000000 OPDEF HALT [JRST 4,] ;DEFINITION FOR DDT
159      254100 000000 OPDEF JRSTF [JRST 2,] ;DEFINITION FOR DDT
160      254500 000000 OPDEF JEN [JRST 12,] ;DEFINITION FOR DDT
161
162      ; *****
163      ; SUBROUTINE INITIALIZATION CALL
164      ; *****
165
166      265000 030011 OPDEF PGMINT [JSP 0,SBINIT] ;SUBROUTINE INITIALIZATION
167
168      ; *****
169      ; HALTING UUO'S (A MORE GRACEFUL HALT THAN SIMPLY USING THE HALT INSTRUCTION).
170      ; *****
171
172      037640 000004 OPDEF FATAL [37B8:15B12:4] ;FATAL PROGRAMMING HALT
173      037600 000004 OPDEF ERRHLT [37B8:14B12:4] ;PROGRAM ERROR HALT
174
175      ; *****
176      ; TERMINAL INPUT UUO'S
177      ; ALWAYS COME FROM THE CONSOLE TERMINAL IN EXEC MODE OR THE
178      ; CONTROLLING TERMINAL (REAL TERMINAL OR PTY) IN USER MODE.
179      ; *****
180
181      037000 000003 OPDEF TTICHR [37B8:0B12:3] ;TTY, INPUT ANY CHARACTER
182      037040 000003 OPDEF TTIIYES [37B8:1B12:3] ;TTY, NORMAL RETURN Y
183      037100 000003 OPDEF TTINO [37B8:2B12:3] ;TTY, NORMAL RETURN N
184      037140 000003 OPDEF TTIOCT [37B8:3B12:3] ;TTY, INPUT OCTAL WORD
185      037200 000003 OPDEF TTIDEC [37B8:4B12:3] ;TTY, INPUT DECIMAL WORD
186      037240 000003 OPDEF TTICNV [37B8:5B12:3] ;TTY, INPUT CONVERTABLE WORD
187      037300 000003 OPDEF TTLOOK [37B8:6B12:3] ;TTY, KEYBOARD CHECK
188      037340 000003 OPDEF TTALTM [37B8:7B12:3] ;TTY, ALT-MODE CHECK
189      037400 000003 OPDEF TTSIXB [37B8:10B12:3] ;TTY, INPUT SIXBIT WORD
190      037440 000003 OPDEF TTYINP [37B8:11B12:3] ;TTY, IMAGE MODE INPUT
191      037500 000003 OPDEF TTICLR [37B8:12B12:3] ;TTY, CLEAR INPUT
  
```

; TERMINAL OUTPUT UUO'S.

192					
193					
194	037000	000000	OPDEF	PNTA	[3788:0812:0] ;PRINT ASCII WORD
195	037000	000001	OPDEF	PNTAF	[3788:0812:1] ;PRINT ASCII WORD FORCED
196	037740	000000	OPDEF	PNTAL	[3788:17812:0] ;PRINT ASCII LINE
197	037740	000001	OPDEF	PNTALF	[3788:17812:1] ;PRINT ASCII LINE FORCED
198	037600	000003	OPDEF	PSIXL	[3788:14812:3] ;PRINT SIXBIT'Z LINE
199	037640	000003	OPDEF	PSIXLF	[3788:15812:3] ;PRINT SIXBIT'Z LINE FORCED
200	037000	000000	OPDEF	PNTMSG	[3788:0812:0] ;PRINT MESSAGE IMMEDIATE
201	037040	000000	OPDEF	PNTMSF	[3788:1812:0] ;PRINT MESSAGE IMMEDIATE FORCED
202	037100	000000	OPDEF	PSIXM	[3788:2812:0] ;PRINT SIXBIT'Z MSG IMMEDIATE
203	037200	000000	OPDEF	PSIXMF	[3788:4812:0] ;PRINT SIXBIT'Z MSG IMM FORCED
204	037000	000000	OPDEF	PNTCI	[3788:0812:0] ;PRINT CHARACTER IMMEDIATE
205	037040	000000	OPDEF	PNTCIF	[3788:1812:0] ;PRINT CHARACTER IMMEDIATE FORCED
206	037500	000000	OPDEF	PNTCHR	[3788:12812:0] ;PRINT CHARACTER
207	037500	000001	OPDEF	PNTCHF	[3788:12812:1] ;PRINT CHARACTER FORCED
208	037040	000000	OPDEF	PNT1	[3788:1812:0] ;PRINT ONE OCTAL DIGIT
209	037040	000001	OPDEF	PNT1F	[3788:1812:1] ;PRINT 1 OCTAL DIGIT FORCED
210	037100	000000	OPDEF	PNT2	[3788:2812:0] ;PRINT TWO OCTAL DIGITS
211	037100	000001	OPDEF	PNT2F	[3788:2812:1] ;PRINT 2 OCTAL DIGITS FORCED
212	037140	000000	OPDEF	PNT3	[3788:3812:0] ;PRINT THREE OCTAL DIGITS
213	037140	000001	OPDEF	PNT3F	[3788:3812:1] ;PRINT THREE OCTAL DIGITS FORCED
214	037200	000000	OPDEF	PNT4	[3788:4812:0] ;PRINT FOUR OCTAL DIGITS
215	037200	000001	OPDEF	PNT4F	[3788:4812:1] ;PRINT FOUR OCTAL DIGITS FORCED
216	037240	000000	OPDEF	PNT5	[3788:5812:0] ;PRINT FIVE OCTAL DIGITS
217	037240	000001	OPDEF	PNT5F	[3788:5812:1] ;PRINT FIVE OCTAL DIGITS FORCED
218	037300	000000	OPDEF	PNT6	[3788:6812:0] ;PRINT SIX OCTAL DIGITS
219	037300	000001	OPDEF	PNT6F	[3788:6812:1] ;PRINT SIX OCTAL DIGITS FORCED
220	037340	000000	OPDEF	PNT7	[3788:7812:0] ;PRINT 7 OCTAL DIGITS
221	037340	000001	OPDEF	PNT7F	[3788:7812:1] ;PRINT 7 OCTAL DIGITS FORCED
222	037440	000000	OPDEF	PNT11	[3788:11812:0] ;PRINT 11 OCTAL DIGITS
223	037440	000001	OPDEF	PNT11F	[3788:11812:1] ;PRINT 11 OCTAL DIGITS FORCED.
224	037400	000000	OPDEF	PNTADR	[3788:10812:0] ;PRINT PHYSICAL ADDRESS
225	037400	000001	OPDEF	PNTADF	[3788:10812:1] ;PRINT PHYSICAL ADDRESS FORCED
226	037600	000000	OPDEF	PNT OCT	[3788:14812:0] ;PRINT FULL WORD OCTAL
227	037600	000001	OPDEF	PNTOTF	[3788:14812:1] ;PRINT FULL WORD OCTAL FORCED
228	037540	000000	OPDEF	PNT HW	[3788:13812:0] ;PRINT OCTAL HALF WORDS, 6 SP 6
229	037540	000001	OPDEF	PNT HWF	[3788:13812:1] ;PRINT OCTAL HALF WORDS, 6 SP 6 FORCED
230	037700	000003	OPDEF	PNT OCS	[3788:16812:3] ;PRINT OCTAL, SUPPRESS LEADING 0'S
231	037740	000003	OPDEF	PNT OCF	[3788:17812:3] ;PRINT OCTAL, SUPPRESS LEADING 0'S FORCED
232	037640	000000	OPDEF	PNT DEC	[3788:15812:0] ;PRINT DECIMAL, SUPPRESS LEADING 0'S
233	037640	000001	OPDEF	PNT DCF	[3788:15812:1] ;PRINT DECIMAL, SUPPRESS LEADING 0'S FORCED
234	037700	000000	OPDEF	PNT DS	[3788:16812:0] ;PRINT DECIMAL, SPACES FOR LD 0'S
235	037700	000001	OPDEF	PNT DSF	[3788:16812:1] ;PRINT DECIMAL, SPACES FOR LD 0'S FORCED


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236 037200 000002 OPDEF PNTNM [37B8!4B12!2] ;PRINT PROGRAM NAME
237 037000 000002 OPDEF PNTSIX [37B8!0B12!2] ;PRINT SIXBIT WORD
238 037040 000002 OPDEF PNTSXF [37B8!1B12!2] ;PRINT SIXBIT WORD FORCED
239 037240 000002 OPDEF DROPDV [37B8!5B12!2] ;CLOSE LOGICAL FILE, USER MODE
240 037100 000002 OPDEF PNTCW [37B8!2B12!2] ;PRINT DF10 CONTROL WORD
241 037140 000002 OPDEF PNTCWF [37B8!3B12!2] ;PRINT DF10 CONTROL WORD FORCED
242 037000 030242 OPDEF PCRL [37B8!0B12!CRLF] ;PRINT CARRIAGE RETURN/LINE FEED
243 037040 030242 OPDEF PCRLF [37B8!1B12!CRLF] ;PRINT CARRIAGE RETURN/LINE FEED FORCED
244 037000 000040 OPDEF PSP [37B8!0B12!40] ;PRINT SPACE
245 037040 000040 OPDEF PSPF [37B8!1B12!40] ;PRINT SPACE FORCED
246 037000 030243 OPDEF PCRL2 [37B8!0B12!CRLF2] ;PRINT CARRIAGE RETURN/LINE FEED (TWICE)
247 037040 030243 OPDEF PCRL2F [37B8!1B12!CRLF2] ;PRINT CARRIAGE RETURN/LINE FEED (TWICE) FORCED
248 037040 000007 OPDEF PBELL [37B8!1B12!7] ;PRINT TTY BELL
249
250 037040 000026 OPDEF PFORCE [37B8!1B12!26] ;PRINT FORCE, CONTROL 0 OVERRIDE
251
252 DEFINE PMSG (ARG),<
253 PSIXM [SIXBIT\ARG'\>
254
255 DEFINE PMSGF (ARG),<
256 PSIXMF [SIXBIT\ARG'\>
257
258 ;SIXBTZ -- MACRO TO GENERATE SIXBIT DATA FOR PRINTING
259 ; CONSERVES CORE OVER ASCII
260
261 DEFINE SIXBTZ (ARG),< [SIXBIT\ARG'\>
262
263 ;CONSOLE SWITCH INPUT UUC.
264 ;READS CONSOLE SWITCHES IF IN EXEC MODE OR ASKS FOR THEM IF
265 ; USER MODE.
266
267 037400 000002 OPDEF SWITCH [37B8!10B12!2] ;INPUT CONSOLE SWITCHES
268
269 ;CLOCK INITIALIZATION UUC - TO SET DESIRED CLOCK OPERATION
270 ;EITHER IGNORE CLOCK, ONLY LET IT TICK OR CAUSE INTERRUPT TO OCCUR.
271
272 037540 000004 OPDEF CLOKOP [37B8!13B12!4] ;CLOCK OPERATION UUC - DP-11 CLOCK
273 037200 000004 OPDEF MTROP [37B8!4B12!4] ;CLOCK OPERATION UUC - 20 METER
274
275 ;KL10 ONLY CACHE OPERATION UUC'S
276
277 037040 000004 OPDEF CINVAL [37B8!1B12!4] ;CACHE INVALIDATE
278 037100 000004 OPDEF CFLUSH [37B8!2B12!4] ;CACHE FLUSH
279 037140 000004 OPDEF CWRTBI [37B8!3B12!4] ;CACHE WRITE-BACK & INVALIDATE

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```

280      ;END OF PASS/PROGRAM UUOS
281
282      ;PERFORMS THE END OF PASS FUNCTIONS. INCREMENT PASS COUNT,
283      ;DECREMENT ITERATION COUNT, CHECK IF FINISHED WITH THIS PROGRAM ETC.
284
285      037500 000004 OPDEF  ENDUO  [37B8!12B12!4] ;UO TO DISPLAY LIGHTS
286      037700 000004 OPDEF  EOPUO  [37B8!16B12!4] ;END OF PROGRAM UO
287
288      ;MEMORY MANAGEMENT UO'S
289      ;UO'S TO PERFORM VARIOUS MEMORY FUNCTIONS. MAPPING, ZEROING, PAGING,
290      ;ADDRESS CONVERSION, ETC...
291
292      037000 000004 OPDEF  MAPMEM [37B8!0B12!4] ;MAP MEMORY
293      037500 000002 OPDEF  MEMZRO [37B8!12B12!2] ;ZERO MEMORY
294      037440 000002 OPDEF  MEMSEG [37B8!11B12!2] ;SETUP MEMORY SEGMENT
295      037540 000002 OPDEF  MAPADR [37B8!13B12!2] ;VIRTUAL TO PHYSICAL ADR CONVERT
296      037640 000002 OPDEF  MAPCNK [37B8!15B12!2] ;MAP MEMORY CHUNK
297      037600 000002 OPDEF  MAPSET [37B8!14B12!2] ;SET KI10 EXEC PAGE MAP
298      037740 000002 OPDEF  MAPPNT [37B8!17B12!2] ;PRINT MEMORY MAP
299
300      ;DEVICE CODE MODIFICATION UO
301      ;ALLOWS THE MODIFICATION OF IOT'S TO ONE DEVICE TO BE CHANGED TO
302      ;IOT'S TO A DIFFERENT DEVICE CODE.
303
304      037340 000002 OPDEF  MODPCU [37B8!7B12!2] ;MODIFY PERHIPERAL CODE, USER
305      037300 000002 OPDEF  MODPCP [37B8!6B12!2] ;MODIFY PERHIPERAL CODE, PROGRAM
306
307      030000 IFNDEF MODDVL,<MODDVL==BEGIN>
308      030000 IFNDEF MGDDVU,<MODDVU==BEGIN>
309
310      ;'DIAMON' FILE SELECTION AND READ UUOS
311
312      037240 000004 OPDEF  FSELECT [37B8!5B12!4] ;FILE SELECTION
313      037300 000004 OPDEF  FREAD  [37B8!6B12!4] ;FILE READ - ASCII DATA
314      037340 000004 OPDEF  FRD36  [37B8!7B12!4] ;FILE READ - 36 BIT DATA
315      037400 000004 OPDEF  FRD8   [37B8!10B12!4] ;FILE READ - 8 BIT DATA
316
317      ;KI10 ONLY UO FOR PRINTING MARGIN VALUES
318
319      037700 000002 OPDEF  PNTMGN [37B8!16B12!2] ;PRINT MARGIN VALUE
320
321      XLIST
322      IFNDEF KLOLD,<LIST

```

```

323      SUBTTL  ERROR HANDLING UDO DEFINITIONS, SEPT 18,1979
324
325      ; *****
326      ; ERROR HANDLER PARAMETERS
327      ; *****
328
329      036000 000000      OPDEF  ERUUD  [36B8]      ;ERROR CALL UUD
330      035000 000000      OPDEF  ERLOOP [35B8]      ;ERROR LOOP, CHECKS PC,REPT,REPT1,ERROR
331      035040 000000      OPDEF  ERLP1  [35B8!1B12] ;ERROR LOOP IF PC'S MATCH
332      035100 000000      OPDEF  ERLP2  [35B8!2B12] ;ERROR LOOP IF ANY ERROR
333      034000 000000      OPDEF  REPTUD [34B8]      ;REPEAT LOOP UUD
334
335      ;THE ERROR HANDLER MACROS
336
337      ;A MACRO TO REPORT AN ERROR AND LOOP
338
339      DEFINE  ERROR  (ADR,FORMAT,CORECT,ACTUAL,F,D,ERR)<
340      ERUUD  FORMAT,[T,,[SIXBIT\F'_\]]      SALL
341      CORECT,ACTUAL
342      [SIXBIT\D'_\]],ERR]
343
344      ERLOOP  ADR      ;IF ERROR, LOOP TO ADR      XALL
345
346      >
347
348      ;A MACRO TO REPORT AN ERROR AND NOT LOOP
349
350      DEFINE  ERROR1 (FORMAT,CORECT,ACTUAL,F,D,ERR)<
351      ERUUD  FORMAT,[T,,[SIXBIT\F'_\]]      SALL
352      CORECT,ACTUAL
353      [SIXBIT\D'_\]],ERR]
354
355      XALL>
356
357      >;END OF KLOLD CONDITIONAL
358
359      XLIST
360      LIST
  
```

```

361 SUBTTL *FIXED* FIXED CONTROL AND DISPATCH STORAGE, SEPT 18,1979
362
363 LOC 30000
364
365 ; *****
366 ; PROGRAM STARTING ADDRESSES
367 ; THESE ADDRESSES CALL VARIOUS SPECIAL START ROUTINES AND OR OPTIONS
368 ; NORMAL START ADDRESS IS 30000 ALL OTHERS ARE SPECIAL. INVOKED BECAUSE
369 ; OF END OF PASS, POWER FAILURE, DDT START, RE-ENTERING(TYPICALLY USER
370 ; MODE), OR ANY NUMBER OF SPECIAL FEATURE TESTS.
371 ; *****
372
373 030000 254 00 1 00 027776 BEGIN: JRST @MODLNK ;STAND-ALONE START
374 030001 254 00 0 00 030674 $START: JRST START ;MODE CHECK STARTING ADDRESS
375
376 030002 254 00 1 00 027774 DIAGMN: JRST @LDLNK ;DIAGNOSTIC MONITOR START
377
378 030003 254 00 1 00 027774 SYSEXR: JRST @LDLNK ;SYSTEM EXERCISER START
379
380 030004 254 00 0 00 030000 SFSTRT: JRST SADR1 ;SPECIAL FEATURE START
381
382 030005 254 00 0 00 030000 PFSTRT: JRST SADR2 ;POWER FAIL RESTART
383
384 030006 254 00 0 00 030000 REENTR: JRST SADR3 ;RE-ENTER START(USUALLY USER MODE ONLY)
385
386 030007 SRTDDT: ;COMMONLY MISTAKEN NAME FOR 'DDTSRT'
387 030007 254 00 1 00 027775 DDTSRT: JRST @DDTLNK ;DDT START
388
389 030010 254 00 0 00 030715 BEGIN1: JRST STARTA ;LOOP START(END OF PASS COMES HERE)
390 030011 254 00 1 00 027777 SBINIT: JRST @SUOLNK ;PMGINT LINKAGE
391 030012 000000 000000 RETURN: 0 ;RETURN ADDRESS STORAGE
392
393 030013 254000 030000 START1: SADR7 ;OPTIONAL STARTING ADR/INSTRUCTIONS
394 030014 254000 030000 START2: SADR8 ;
395 030015 254000 030000 START3: SADR9 ;
396 030016 254000 030000 START4: SADR10 ;
397 030017 254000 030000 START5: SADR11 ;
    
```



```

398
399
400
401
402 030020 444653 414400
403 030021 546064 0J0000
404 030022 000000 000000
405 030023 000000 000000
406 030024 000000 001000
407 030025 000000 030701
408 030026 000000 000002
409 030027 000000 030000
410 030030 000000 030000
411 030031 777777 777777
412 030032 777777 777777
413 030033 000000 000000
414 030034 777777 777777
415 030035 000000 000000
416 030036 000000 000000
417
418
419
420
421
422 030037 000000 000000
423 030040 000000 000000
424 030041 000000 000000
425 030042 777777 777777
426 030043 000000 000000
427 030044 000000 000000
428 030045 000000 000000
429 030046 000000 000000
430 030047 000000 000000
431 030050 000000 000000
432 030051 000000 000000
433 030052 000000 000000
434 030053 000000 000000
435 030054 000000 000000
436 030055 000000 000000
437 030056 000000 000000
    
```

```

: *****
: PROGRAM FIXED PARAMETER AREA
: *****
    
```

```

PNTNAM: PAREA3      ;SIXBIT PROGRAM NAME
PNTXT: PAREA4       ;SIXBIT PROGRAM EXTENSION
RANDBS: PAREA1      ;RANDOM BASE NUMBER
SWTEXR: PAREA2      ;SYSTEM EXERCISER SWITCHES
ITRCNT: ITERAT      ;PROGRAM ITERATIONS
$PNAME: PGMNAM      ;POINTER TO PROGRAMS NAME
$PVER: MCNVER,,DECVER ;MCN & DEC VERSION LEVEL
$MODVL: MODDVL      ;DEVICE CODE CHANGE LOWER LIMIT
$MODVU: MODDVU      ;DEVICE CODE CHANGE UPPER LIMIT
$EMODE: IFNDEF EXCASB,<0> IFDEF EXCASB,<-1> ;EXEC ALLOWED
$UMODE: IFNDEF USRASB,<0> IFDEF USRASB,<-1> ;USER ALLOWED
$DSKUP: IFNDEF DSKUPD,<0> IFDEF DSKUPD,<-1> ;DISK UPDATE MODE
$MMAP: IFNDEF MEMMAP,<0> IFDEF MEMMAP,<-1> ;ALLOW MEMORY RTNS
PAREA7: PAREA5      ;OPTIONAL PARAMETER
PAREA8: PAREA6      ;OPTIONAL PARAMETER
    
```

```

: *****
: PROGRAM VARIABLE PARAMETER AREA
: *****
    
```

```

USER: 0      ; 0 = EXEC, -1 = USER MODE FLAG
KAIFLG: 0    ;PROCESSOR TYPE, 0 = KA10, -1 = KI10
KLFLG: 0    ;PROCESSOR TYPE, 0 = KA/KI, -1 = KL10
MONFLG: -1   ;DIAG MONITOR SPECIAL USER FLAG
MONCTL: 0    ;DIAG MON/SYS EXR FLAG
MONTEN: 0    ;-1= LOADED BY 10
CLOCKF: 0    ;CLOCK TICKED FLAG
CONSW: 0     ;CONSOLE SWITCH SETTINGS
PASCNT: 0    ;PROGRAM PASS COUNT
RUNFLG: 0    ;PROGRAM RUN FLAG
TESTPC: 0    ;SUBTEST PC
ERRPC: 0     ;ERROR PC
ERRTLS: 0    ;ERROR TOTALS
TICKS: 0     ;PROGRAM RUNNING TIME
MARGIN: 0    ;KI10 MARGIN WORD VALUE
$ONETM: 0    ;SUBROUTINE INITIALIZATION FLAG
    
```

```

438                                     : *****
439                                     : SPECIAL PROGRAM DISPATCH ADDRESSES
440                                     : *****
441
442 030057 037 12 0 00 000004    BEGEND: ENDUO          :END OF PASS
443 030060 254 00 0 00 030010    $BEND1: JRST          :KEEP RUNNING PROGRAM
444 030061 037 16 0 00 000004    $BEND2: EOPUO          :END OF PROGRAM - NO RETURN
445 030062 254000 030000    CNTLC: SADR5          :CONTROL C XFER ADDRESS
446 030063 254000 030000    ALTMGO: SADR6          :ALTMODE XFER ADDRESS
447 030064                                CPOPJ1:          :SKIP RETURN
448 030064 350 00 0 17 000000    UOOSKP: ADS      (P)    :SKIP RETURN FROM UO
449 030065                                CPOPJ:          :NON-SKIP REGULAR RETURN
450 030065 263 17 0 00 000000    UOEXT: RTN          :UO RETURN
451 030066 255 00 0 00 000000    UUORTN: JFCL          :ADDITIONAL USERS UO ROUTINE
452 030067 255 00 0 00 000000    $UORTX: JFCL          :ADDITIONAL UO LINKAGE
453 030070 255 00 0 00 000000    $UOER: JFCL          :INITED AS (JRST $UOERX)
454 030071 255 00 0 00 000000    $ITRHL: JFCL          :ADDITIONAL INTERRUPT LINKAGE
455 030072 255 00 0 00 000000    $ITRX1: JFCL          :
456 030073 255 00 0 00 000000    $USRHL: JFCL          :
457 030074 255 00 0 00 000000    $RSRTX: JFCL          :ADDITIONAL POWER FAIL LINKAGE
458 030075 255 00 0 00 000000    $RSRTY: JFCL          :
459 030076 255 00 0 00 000000    RESRT1: JFCL          : INITED AS (JRST RESRTX)
460 030077 255 00 0 00 000000    RESRT2: JFCL          :
461 030100 255 00 0 00 000000    $PARER: JFCL          :ADDITIONAL PARITY ERROR LINKAGE
462 030101 255 00 0 00 000000    ERMORE: JFCL          :ADDITIONAL ERROR HANDLER LINKAGE
463 030102 254 04 0 00 030102    HALT                :IMPROPER TRANSFER HALT
464
465 030103 000000 000000    $PSHER: 0                :INITED AS (JRST PSHERR)
466 030104 000000 000000    ITRCH1: 0                :PC & FLAGS OF CURRENT INTERRUPT
467 030105 000000 000000    0                        :INITED AS (JRST $ITRC1)
468
469                                     : *****
470                                     : PROCESSOR CONTROL STORAGE
471                                     : *****
472
473 030106 000000 000000    $ACCO: 0                : INTERRUPT SAVED ACO
474 030107 000000 000000    $SVPI: 0                : INTERRUPT SAVED PI
475 030110 000000 000000    $SVAPR: 0               : INTERRUPT SAVED APR
476 030111 000000 000000    $VPAG: 0                : INTERRUPT SAVED PAG (DATAI)
477 030112 000000 000000    $SPAG1: 0               : INTERRUPT SAVED PAG (CONI)
478
479 030113 000000 000000    $SVUO: 0                : CURRENT USERS UO
480 030114 000000 000000    $SVUPC: 0               : PC OF CURRENT USERS UO
481
482 030115 000000 000000    REPTU: 0                : REPEAT UO ITERATIONS
483 030116 000000 000000    SCOPE: 0                : ERROR HANDLER SCOPE LOOP FLAG
484 030117 000000 000000    %CORFLG: 0              : " CORRECT FLAG
485 030120 000000 000000    %COREC: 0              : " CORRECT DATA
486 030121 000000 000000    %ACTFL: 0              : " ACTUAL FLAG
487 030122 000000 000000    %ACTUL: 0              : " ACTUAL DATA
488 030123 000000 000000    %DISCR: 0              : " DISCREPENCY DATA
    
```

489
 490
 491
 492
 493
 494 030124 030070 030070
 495 030125 030070 030070
 496 030126 030070 030070
 497 030127 030070 030070
 498 030130 030070 030070
 499 030131 030070 030070
 500 030132 030070 030070
 501 030133 030070 030070
 502 030134 030070 030070
 503 030135 030070 030070
 504 030136 030070 030070
 505 030137 030070 030070
 506 030140 030070 030070
 507 030141 030070 030070
 508
 509
 510
 511
 512
 513 030142 000000 000000
 514 030143 000000 000000
 515 030144 000000 000000
 516 030145 000000 000000
 517 030146
 518
 519
 520
 521
 522
 523 030217 000000 000000
 524 030220 000000 000000
 525 030221 000000 000000
 526 030222 000000 000000
 527 030223 000000 000000
 528 030224 000000 000000
 529 030225 000000 000000
 530 030226 000000 000000
 531 030227 000000 000000
 532 030230 000000 000000
 533 030231 000000 000000
 534 030232 000000 000000
 535 030233 000000 000000
 536 030234 000000 000000
 537 030235 000000 000000
 538 030236 000000 000000
 539 030237 000000 000000
 540 030240 000000 000000
 541 030241 000000 000000

```

; *****
;UUO DISPATCH TABLE
; *****
      XLIST
      LIST
UUODIS: LUU01,, $UUOER
        LUU03,, LUU02
        LUU05,, LUU04
        LUU07,, LUU06
        LUU011,, LUU010
        LUU013,, LUU012
        LUU015,, LUU014
        LUU017,, LUU016
        LUU021,, LUU020
        LUU023,, LUU022
        LUU025,, LUU024
        LUU027,, LUU026
        LUU031,, LUU030
        LUU033,, LUU032

; *****
;MEMORY MANAGMENT STORAGE
; *****

DF22F: 0          ;DF10 CONTROL FLAG, 0 = 18, -1 = 22 BIT
MAPNEW: 0         ;MEMORY MAPPING CONTROL FLAG, -1 = 4096K MAPPING
MEMTOT: 0         ;TOTAL MEMORY SIZE IN K (1024.)
MEMLOW: 0         ;LOWEST USABLE MEMORY
MEMSIZ: BLOCK ^D41 ;MEMORY SEGMENT POINTER TABLE

; *****
;PRINT CONTROL STORAGE
; *****

PNTFLG: 0          ;PRINT FLAG, -1 WHILE IN PRINT ROUTINE
PNTENB: 0          ;PRINT ENABLE
PDISF: 0           ;PRINT DISABLED FLAG
PNTINH: 0          ;INHIBIT PRINT INPUT CHECKS
PNTSPC: 0          ;PRINT SPACE CONTROL
OPTIME: 0          ;TYPE-IN WAIT TIME
$TWCNT: 0          ;TIME WAITED
$DVOFF: 0          ;LOGICAL DEVICE INITED FLAG
TTYFIL: 0          ;TTY EXEC FILLERS FLAG
TTYSPD: 0          ;TTY EXEC BAUD RATE
$TTCHR: 0          ;ACTUAL TYPED IN CHAR
$CHRIN: 0          ;UPPER CASED & PARITY STRIPPED CHAR
$TYPNB: 0          ;TYPED IN NUMBER
$CRLF: 0           ;FREE CR/LF FLAG
$TABF: 0           ;TAB CONVERSION FLAG
$FFF: 0            ;FORM FEED CONVERSION FLAG
$VTF: 0            ;VERTICAL TAB CONVERSION FLAG
$URLFF: 0          ;USER LF FILLERS
$USRCRF: 0         ;USER CR FILLERS
    
```



```

542      : *****
543      : THE FOLLOWING MISCELLANEOUS PRINT CHARACTERS ARE INCLUDED
544      : TO FACILITATE PRINTING AND ARE CALLED AS FOLLOWS:
545      :     MOVEI    NAME
546      :     PNTA     ;OR PNTAF
547      : *****
548
549 030242 CRLF:  ASCII/
550 030242 015 012 000 000 000 /
551 030243 CRLF2: ASCII/
552
553 030243 015 012 015 012 000 /
554 030244 054 000 000 000 000 COMMA:  ASCII/./
555 030245 056 000 000 000 000 PERIOD: ASCII/./
556 030246 040 000 000 000 000 SPACE:  ASCII/ /
557 030247 011 000 000 000 000 TAB:    ASCII/ /
558 030250 MINUS:
559 030250 055 000 000 000 000 HYPEN:  ASCII/~ /
560 030251 053 000 000 000 000 PLUS:   ASCII/+ /
561 030252 052 000 000 000 000 AST:   ASCII/* /
562 030253 100 000 000 000 000 AT$IN: ASCII/@ /
563 030254 050 000 000 000 000 LFP:   ASCII/( /
564 030255 051 000 000 000 000 RTP:   ASCII)/ /
565 030256 007 000000000000 BELL:  BYTE (7) 007
566 030257 077 000 000 000 000 QUEST:  ASCII/? /
567 030260 057 000 000 000 000 SLASH:  ASCII!/ /
568 030261 044 000 000 000 000 DOLLAR: ASCII/$ /
569 030262 000000 000012 RADIX:  ^D10 ;DECIMAL PRINT RADIX
570 030263 000000 000040 RADLSP: 40 ;DECIMAL PRINT LEADING CHAR
571 030264 000000 000012 RADLSC: ^D10 ;DECIMAL PRINT LEADING CHAR COUNT
572
573      : *****
574      : USER MODE OUTPUT FILE INFORMATION
575      : *****
576
577 030265 $OBUF:  BLOCK 3 ;LOGICAL FILE OUTPUT BUFFER HEADER
578 030270 60 62 51 56 64 00 $OUTNM: SIXBIT /PRINT/ ;FILE NAME
579 030271 60 56 64 00 00 00 $OUTEX: SIXBIT /PNT/ ;FILE NAME EXTENSION
580 030272 BLOCK 2
581
582      : *****
583      : DISK UPDATE MODE FILE INFORMATION
584      : *****
585
586 030274 $IBUF:  BLOCK 3
587 030277 60 62 51 56 64 00 $INNM:  SIXBIT /PRINT/
588 030300 60 56 64 00 00 00 $INEXT: SIXBIT /PNT/
589 030301 BLOCK 2
    
```



```

590      ; *****
591      ;PUSHDOWN LIST CONTROL INFORMATION
592      ; *****
593
594 030303 777577 030303  PLIST: PLIST-PLISTE,,PLIST
595 030304          000000  PLISTS: BLOCK 200
596 030504 000000 000000  PLISTE: 0          ;END OF PUSHDOWN LIST
597
598      ; *****
599      ;POWER LINE CLOCK FREQUENCY FLAG
600      ; *****
601
602 030505 000000 000000  CYCL60: 0          ;0 = 60, -1 = 50 CYCLE
603
604      ; *****
605      ;KL10 CACHE CONTROL FLAGS
606      ; *****
607
608 030506 000000 000000  CSHFLG: 0          ;ALLOW CACHE IF 0
609 030507 000000 000000  CSHMEM: 0         ;CACHE MEMORY SEGMENTS IF 0
610
611      ; *****
612      ;NUMBER INPUT DIGIT FLAG
613      ; *****
614
615 030510 000000 000000  TTNBRF: 0          ;-1 IF ANY DIGIT TYPED
616
617      ; *****
618      ;KL10 & KI10 'INHPAG' SWITCH PAGING PREVENTION
619      ; *****
620
621 030511 000000 000000  PVPAGI: 0          ;IF NON-ZERO, OVERRIDE 'INHPAG' SWITCH ACTION
622
623      ; *****
624      ;ERROR REPORTING ROUTINE ADDITIONAL USERS CONTROL INSTRUCTIONS
625      ; *****
626
627 030512 000000 000000  %ERHI1: 0          ;IF NON-ZERO, XCT'D AT START OF %ERUUO
628 030513 000000 000000  %ERHI2: 0          ;IF NON-ZERO, XCT'D AT END OF %ERUUO
629 030514 000000 000000  %ERHI3: 0          ;IF NON-ZERO, XCT'D AFTER 'PC' OF %ERUUO
630
631      ; *****
632      ;SPECIAL USERS UO INTERCEPT INSTRUCTION
633      ; *****
634
635 030515 000000 000000  $$UUO: 0          ;IF NON-ZERO, XCT'D AT START OF $UORTN
    
```

```

636      : *****
637      : USER MODE MONITOR TYPE FLAG
638      : *****
639
640 030516 000000 000000 MONTYP: 0      ;0 = TOPS10, -1 = TOPS20
641
642      : *****
643      : SPECIAL USERS MUUO INTERCEPT INSTRUCTION
644      : *****
645
646 030517 000000 000000 $$MUUO: 0      ;IF NON-ZERO, XCT'D AT START OF MUUOER
647
648      : *****
649      : SPECIAL USERS USER MODE OUTPUT ERROR INTERCEPT INSTRUCTION
650      : *****
651
652 030520 000000 000000 $$OUTER:0      ;IF NON-ZERO, XCT'D AT END OF USER MODE ERROR
653
654      : *****
655      : 'SWITCH' CALL USAGE CONTROL
656      : *****
657
658 030521 000000 000000 $$TOGGLE:0      ;IF NON-ZERO, USE C(CONSW) FOR SWITCHES
659
660      : *****
661      : SPECIAL USERS ALTMODE SWITCH CALL INTERCEPT INSTRUCTIONS
662      : *****
663
664 030522 000000 000000 $$TAX1: 0      ;IF NON-ZERO, XCT'D AT START OF ALTMODE SWITCH CALL
665 030523 000000 000000 $$TAX2: 0      ;IF NON-ZERO, XCT'D AT END OF ALTMODE SWITCH CALL
666
667      : *****
668      : SM10 (KS-10) PROCESSOR TYPE FLAG
669      : *****
670
671 030524 000000 000000 SM10: 0      ;IF -1 THIS IS A KS-10
672
673      : *****
674      : RIGHT HALF SWITCHES PROMPT TABLE ADDRESS
675      : *****
676
677 030525 000000 000000 SWPTAB: 0      ;0 = NO PROMPT, ADR = ADR OF SIXBIT PROMPT TABLE
678
679      : *****
680      : SPECIAL FUTURE EXPANSION ROOM
681      : *****
682
683      : *****
684      : END OF FIXED STORAGE
685      : *****
686
687 030577      LOC 30577
688 030577 000000 000000 ENDFIX: 0      ;END OF FIXED STORAGE
    
```

```

689          SUBTTL *SPCCPU* SPECIAL BASIC CPU PROCESSOR CONTROL, 26-FEB-76
690
691          ;NEW DEFINITIONS USED BY THE KL10 SUBROUTINE PACKAGE
692
693          000000      ACO=      0
694          030000      DIAGNOS=30000      ;PDP-10 DIAGNOSTIC START ADDRESS
695          010000      DDT=      10000      ;PDP-10 DDT START ADDRESS
696          020000      DIAMON= 20000      ;PDP-10 DIAMON LOADER START ADDRESS
697          020000      DONG11= 1B22      ;11 DOORBELL (FROM THE 10)
698
699          ;DTE20 DEVICE CODES
700
701          000200      DTE==      200      ;DTE0
702          000204      DTE0==      204
703          000204      DTE1==      204
704          000210      DTE2==      210
705          000214      DTE3==      214
706
707          ;KL10 EPT COMMUNICATION AREA
708
709          000440      $STD=      440      ;PDP-10 DIAGNOSTIC START ADDRESS
710          000441      $DDT=      441      ;PDP-10 DDT START ADDRESS
711          000442      $STL=      442      ;PDP-10 LOADER START ADDRESS
712          000443      $STM=      443      ;PDP-10 MONITOR START ADDRESS
713
714          000444      $DTFLG= 444      ;DTE20 OPERATION COMPLETE FLAG
715          000445      $DTCLK= 445      ;DTE20 CLOCK INTERRUPT FLAG
716          000446      $DTCI= 446      ;DTE20 CLOCK INTERRUPT INSTRUCTION
717          000447      $DTT11= 447      ;DTE20 10 TO 11 ARGUMENT
718          000450      $DTF11= 450      ;DTE20 11 TO 10 ARGUMENT
719          000451      $DTCMD= 451      ;DTE20 TO 11 COMMAND WORD
720          000452      $DTSEQ= 452      ;DTE20 OPERATION SEQUENCE NUMBER
721          000453      $DTOPR= 453      ;DTE20 OPERATIONAL DTE #
722          000454      $DTCHR= 454      ;DTE20 LAST TYPED CHARACTER
723          000455      $DTMTD= 455      ;DTE20 MONITOR TTY OUTPUT COMPLETE FLAG
724          000456      $DTMTI= 456      ;DTE20 MONITOR TTY INPUT FLAG
725
726          000457      $DTSWR= 457      ;DTE20 CONSOLE SWITCH REGISTER
  
```

Line	Address	Op	Op2	Op3	Op4	Op5	Op6	Op7	Op8	Op9	Op10	Op11	Op12	Op13	Op14	Op15	Op16	Op17	Op18	Op19	Op20	Op21	Op22	Op23	Op24	Op25	Op26	Op27	Op28	Op29	Op30	Op31	Op32	Op33	Op34	Op35	Op36	Op37	Op38	Op39	Op40	Op41	Op42	Op43	Op44	Op45	Op46	Op47	Op48	Op49	Op50	Op51	Op52	Op53	Op54	Op55	Op56	Op57	Op58	Op59	Op60	Op61	Op62	Op63	Op64	Op65	Op66	Op67	Op68	Op69	Op70	Op71	Op72	Op73	Op74	Op75	Op76	Op77	Op78	Op79	Op80	Op81	Op82	Op83	Op84	Op85	Op86	Op87	Op88	Op89	Op90	Op91	Op92	Op93	Op94	Op95	Op96	Op97	Op98	Op99	Op100	Op101	Op102	Op103	Op104	Op105	Op106	Op107	Op108	Op109	Op110	Op111	Op112	Op113	Op114	Op115	Op116	Op117	Op118	Op119	Op120	Op121	Op122	Op123	Op124	Op125	Op126	Op127	Op128	Op129	Op130	Op131	Op132	Op133	Op134	Op135	Op136	Op137	Op138	Op139	Op140	Op141	Op142	Op143	Op144	Op145	Op146	Op147	Op148	Op149	Op150	Op151	Op152	Op153	Op154	Op155	Op156	Op157	Op158	Op159	Op160	Op161	Op162	Op163	Op164	Op165	Op166	Op167	Op168	Op169	Op170	Op171	Op172	Op173	Op174	Op175	Op176	Op177	Op178	Op179	Op180	Op181	Op182	Op183	Op184	Op185	Op186	Op187	Op188	Op189	Op190	Op191	Op192	Op193	Op194	Op195	Op196	Op197	Op198	Op199	Op200	Op201	Op202	Op203	Op204	Op205	Op206	Op207	Op208	Op209	Op210	Op211	Op212	Op213	Op214	Op215	Op216	Op217	Op218	Op219	Op220	Op221	Op222	Op223	Op224	Op225	Op226	Op227	Op228	Op229	Op230	Op231	Op232	Op233	Op234	Op235	Op236	Op237	Op238	Op239	Op240	Op241	Op242	Op243	Op244	Op245	Op246	Op247	Op248	Op249	Op250	Op251	Op252	Op253	Op254	Op255	Op256	Op257	Op258	Op259	Op260	Op261	Op262	Op263	Op264	Op265	Op266	Op267	Op268	Op269	Op270	Op271	Op272	Op273	Op274	Op275	Op276	Op277	Op278	Op279	Op280	Op281	Op282	Op283	Op284	Op285	Op286	Op287	Op288	Op289	Op290	Op291	Op292	Op293	Op294	Op295	Op296	Op297	Op298	Op299	Op300	Op301	Op302	Op303	Op304	Op305	Op306	Op307	Op308	Op309	Op310	Op311	Op312	Op313	Op314	Op315	Op316	Op317	Op318	Op319	Op320	Op321	Op322	Op323	Op324	Op325	Op326	Op327	Op328	Op329	Op330	Op331	Op332	Op333	Op334	Op335	Op336	Op337	Op338	Op339	Op340	Op341	Op342	Op343	Op344	Op345	Op346	Op347	Op348	Op349	Op350	Op351	Op352	Op353	Op354	Op355	Op356	Op357	Op358	Op359	Op360	Op361	Op362	Op363	Op364	Op365	Op366	Op367	Op368	Op369	Op370	Op371	Op372	Op373	Op374	Op375	Op376	Op377	Op378	Op379	Op380	Op381	Op382	Op383	Op384	Op385	Op386	Op387	Op388	Op389	Op390	Op391	Op392	Op393	Op394	Op395	Op396	Op397	Op398	Op399	Op400	Op401	Op402	Op403	Op404	Op405	Op406	Op407	Op408	Op409	Op410	Op411	Op412	Op413	Op414	Op415	Op416	Op417	Op418
------	---------	----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------

LOC	\$\$\$LOC	;	RESET CURRENT LOCATION
768 030600			
769			
770			
771			
772 030600	402 00 0 00 030037	\$\$\$START: SETZM	USER
773 030601	265 00 0 00 030602	JSP	0, +1
774 030602	603 00 0 00 010000	TLNE	0, USERF
775 030603	476 00 0 00 030037	SETOM	USER
776 030604	336 00 0 00 030042	SKIPN	MONFLG
777 030605	402 00 0 00 030037	SETZM	USER
778 030606	332 00 0 00 030037	SKIPE	USER
779 030607	254 00 0 00 030674	JRST	START
780			
781 030610	336 00 0 00 030044	\$\$\$STKIL: SKIPN	MONTEN
782 030611	476 00 0 00 030024	SETOM	ITRCNT
783 030612	402 00 0 00 030041	SETZM	KLFLG
784 030613	200 01 0 00 034417	MOVE	1, [1, , 1]
785 030614	251 01 0 00 000001	BLT	1, 1
786 030615	316 01 0 00 034417	CAMN	1, [1, , 1]
787 030616	254 00 0 00 030674	JRST	START
788			
789 030617	402 00 0 00 000444	\$\$\$STKL: SETZM	\$DITFLG
790 030620	402 00 0 00 000445	SETZM	\$DITCLK
791 030621	200 00 0 00 000453	MOVE	\$DITOPR
792 030622	436 00 0 00 030657	ORM	\$\$\$DTE0
793 030623	436 00 0 00 030670	ORM	\$\$\$DTE2
794 030624	476 00 0 00 030041	SETOM	KLFLG
795 030625	254 00 0 00 030674	JRST	START
796			
797 030626	200 00 0 00 034420	\$\$\$SPEC: MOVE	[JRST STARTA]
798 030627	202 00 0 00 030633	MOVEM	\$\$\$PB1
799 030630	254 00 0 00 030674	JRST	START

```

800 ;SPECIAL 'BEGEND' ROUTINE
801
802 030631 350 00 0 00 030047 $SPBEND: AOS PASCNT ;INCREMENT PASS COUNT
803 030632 370 00 0 00 030024 ;SOS ITRCNT ;DECREMENT ITERATION COUNT
804 030633 336 00 0 00 030037 $SPB1: SKIPN USER
805 030634 254 00 0 00 030642 JRST $SPBEX ;EXEC MODE
806
807 030635 332 00 0 00 030024 $SPBUS: SKIPE ITRCNT ;USER MODE, COMPLETED ?
808 030636 254 00 0 00 030715 JRST STARTA ;NO, KEEP RUNNING
809 030637 336 00 0 00 030044 SKIPN MONTEN ;DONE, LOADED BY 'DIAMON' ?
810 030640 047 00 0 00 000012 EXIT ;NO, RETURN TO MONITOR
811 030641 254 00 1 00 030012 JRST @RETURN ;YES, RETURN TO 'DIAMON'
812
813 030642 332 00 0 00 030041 $SPBEX: SKIPE KLFLG
814 030643 254 00 0 00 030650 JRST $SPBKL ;KL10 & EXEC
815 030644 7 004 14 0 00 030024 DATAO PI, ITRCNT ;KL10 & EXEC, DISPLAY ITER COUNT
816 030645 332 00 0 00 030024 SKIPE ITRCNT
817 030646 254 00 0 00 030715 JRST STARTA ;NOT COMPLETED YET
818 030647 254 00 1 00 030012 JRST @RETURN ;DONE
819
820 030650 336 00 0 00 030024 $SPBKL: SKIPN ITRCNT
821 030651 254 00 0 00 030663 JRST $SPBKL ;KL10, EXEC & COMPLETED
822
823 030652 335 00 0 00 030043 SKIPGE MONCTL
824 030653 254 00 0 00 030715 JRST STARTA ;'DIAMON' CONTROL
825 030654 201 00 0 00 000404 MOVEI 0,404 ;NOTIFY PDP-11 OF END OF PASS
826 030655 202 00 0 00 000451 MOVEM 0,$DTCMD
827 030656 402 00 0 00 000444 SETZM $DTFLG
828 030657 7 200 20 0 00 020000 $$DTE0: CONO DTE,DONG11
829 030660 336 00 0 00 000444 SKIPN $DTFLG ;WAIT TILL 11 RESPONDS
830 030661 254 00 0 00 030660 JRST -1
831 030662 254 00 0 00 030715 JRST STARTA ;KEEP RUNNING
832
833 ;SPECIAL KL10 COMPLETED ROUTINE
834
835 030663 332 00 0 00 030044 $SPKLD: SKIPE MONTEN
836 030664 254 00 1 00 030012 JRST @RETURN ;LOADED BY 'DIAMON'
837
838 030665 201 00 0 00 000403 MOVEI 0,403 ;NOTIFY PDP-11 OF COMPLETION
839 030666 202 00 0 00 000451 MOVEM 0,$DTCMD
840 030667 402 00 0 00 000444 SETZM $DTFLG
841 030670 7 200 20 0 00 020000 $$DTE2: CONO DTE,DONG11
842 030671 336 00 0 00 000444 SKIPN $DTFLG ;SHOULD NEVER HAPPEN
843 030672 254 00 0 00 030671 JRST -1 ;11 NEVER RETURNS ON END OF PROGRAM
844 030673 254 04 0 00 030000 HALT BEGIN ;IF IT DOES, HALT.

```

```
845 SUBTTL DIAGNOSTIC SECTION
846
847 030674 336 00 0 00 030037 START: SKIPN USER
848 030675 254 00 0 00 030715 JRST STARTA
849
850 030676 331 00 0 00 030043 SKIPL MONCTL
851 030677 051 03 0 00 030701 TTCALL 3,PGMNAM
852 030700 254 00 0 00 030715 JRST STARTA
853
854 030701 PGMNAM: ASCIZ/
855 030701 015 012 104 105 103 DECSYSTEM KL10 BASIC INSTRUCTION DIAGNOSTIC (4) [DFKAD]
856 030702 123 131 123 124 105
857 030703 115 040 113 114 061
858 030704 060 040 102 101 123
859 030705 111 103 040 111 116
860 030706 123 124 122 125 103
861 030707 124 111 117 116 040
862 030710 104 111 101 107 116
863 030711 117 123 124 111 103
864 030712 040 050 064 051 040
865 030713 133 104 106 113 101
866 030714 104 135 015 012 000 /
867
868 ;Basic instruction test (4)
869 ;The test is designed for initial debugging of
870 ;Processor hardware and to detect (solid) failures
871 ;In the field.
872
873 030715 254 00 0 00 030716 STARTA: JRST .+1
```

```

SUBTTL  TEST OF AC HARDWARE AND INDEX REGISTERS

;Note:  an "*" in the comment field of an instruction indicates that
;        It is the tested instruction.

;*****

;This test verifies that ac1 is accessible
;In this case, ac1 is preloaded with 1.
;C(ac1) is then checked for a1.  this test passes if c(ac1)=1.
;If this test fails, the ac hardware is probably faulty.

C100:    SETZ                      ;Clear ac0
          MOVEI      1,1           ;Preload ac1 umth 1
          CAIE       1,1           ;Pass if c(ac1)=1
          STOP^
          HALT       .+1           ;Test failed if program halts here
          JUMPA      .+1           ;To loop change this instruction^

;*****

;This test verifies that ac2 is accessible.
;In this case, ac2 is preloaded with 2.
;C(ac2) is then checked for 2.  this test passes if c(ac2)=2.
;If this test fails, the ac hardware is probably faulty.

C200:    MOVEI      2,2           ;Preload ac2 with 2
          CAIE       2,2           ;Pass if c(ac2)=2
          STOP^
          HALT       .+1           ;Test failed if program halts here
          JUMPA      .+1           ;To loop change this instruction^

;*****

```



```

908 ;This test verifies that ac4 is accessable.
909 ;In this case, ac4 is preloaded with 4.
910 ;C(ac4) is then checked for 4. this test passes if c(ac4)=4.
911 ;If this test fails, the ac hardware is probably faulty.
912
913 030727 201 04 0 00 000004 C300: MOVEI 4,4 ;Preload ac4 with 4
914 030730 302 04 0 00 000004 CAIE 4,4 ;Pass if c(ac4)=4
915 STOP^
916 030731 254 04 0 00 030732 HALT .+1 ;Test failed if program halts here
917 030732 324 00 0 00 030733 JUMPA .+1 ;To loop change this instruction^
918
919 ;*****
920
921 ;This test verifies that ac10 is accessable.
922 ;In this case, ac10 is preloaded with 10.
923 ;C(ac10) is then checked for 10. this test passes if c(ac10)=10.
924 ;If this test fails, the ac hardware is probably faulty.
925
926 030733 201 10 0 00 000010 C400: MOVEI 10,10 ;Preload ac10 with 10
927 030734 302 10 0 00 000010 CAIE 10,10 ;Pass if c(ac10)=10
928 STOP^
929 030735 254 04 0 00 030736 HALT .+1 ;Test failed if program halts here
930 030736 324 00 0 00 030737 JUMPA .+1 ;To loop change this instruction^
931
932 ;*****

```



```

977          000020          ZZ=20
978
979          REPEAT ^D16,<
980          ;This test verifies that all acs exist. first, each ac is
981          ;Preloaded with its own address. then, the contents of each
982          ;Ac is checked for its address. if any ac does not contain
983          ;Its address, this test fails.
984
985          SN=SN+1
986          ZZ=ZZ-1
987          CAIE    ZZ,ZZ          ;Check that each ac contains its own address
988          STOP
989          ;In case of failure, loop to 'c500' address
990
991          ;*****
992          >
993
994          ;This test verifies that all acs exist. first, each ac is
995          ;Preloaded with its own address. then, the contents of each
996          ;Ac is checked for its address. if any ac does not contain
997          ;Its address, this test fails.
998
999          000501
1000         000017
1001 030757 302 17 0 00 000017          ZZ=ZZ-1
1002                                     CAIE    ZZ,ZZ          ;Check that each ac contains its own address
1003                                     STOP^
1004 030760 254 04 0 00 030761          HALT    .+1          ;Test failed if program halts here
1005 030761 324 00 0 00 030762          JUMPA   .+1          ;To loop change this instruction^
1006                                     ;In case of failure, loop to 'c500' address
1007
1008          ;*****
1009
1010          ;This test verifies that all acs exist. first, each ac is
1011          ;Preloaded with its own address. then, the contents of each
1012          ;Ac is checked for its address. if any ac does not contain
1013          ;Its address, this test fails.
1014
1015          000502
1016         000016
1017 030762 302 16 0 00 000016          ZZ=ZZ-1
1018                                     CAIE    ZZ,ZZ          ;Check that each ac contains its own address
1019                                     STOP^
1020 030763 254 04 0 00 030764          HALT    .+1          ;Test failed if program halts here
1021 030764 324 00 0 00 030765          JUMPA   .+1          ;To loop change this instruction^
1022                                     ;In case of failure, loop to 'c500' address
1023
1024          ;*****
1025
1026          ;This test verifies that all acs exist. first, each ac is
1027          ;Preloaded with its own address. then, the contents of each
1028          ;Ac is checked for its address. if any ac does not contain
1029          ;Its address, this test fails.
1030
1031          000503          SN=SN+1
    
```

```

1032          000015          ZZ=ZZ-1
1033 030765 302 15 0 00 000015      CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1034          STOP^
1035 030766 254 04 0 00 030767      HALT      .+1          ;Test failed if program halts here
1036 030767 324 00 0 00 030770      JUMPA     .+1          ;To loop change this instruction^
1037                                     ;In case of failure, loop to 'c500' address
1038
1039          ;*****
1040
1041          ;This test verifies that all acs exist. first, each ac is
1042          ;Preloaded with its own address. then, the contents of each
1043          ;Ac is checked for its address. if any ac does not contain
1044          ;Its address, this test fails.
1045
1046          000504
1047          000014          SN=SN+1
1048          ZZ=ZZ-1
1049 030770 302 14 0 00 000014      CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1050          STOP^
1051 030771 254 04 0 00 030772      HALT      .+1          ;Test failed if program halts here
1052 030772 324 00 0 00 030773      JUMPA     .+1          ;To loop change this instruction^
1053                                     ;In case of failure, loop to 'c500' address
1054
1055          ;*****
1056
1057          ;This test verifies that all acs exist. first, each ac is
1058          ;Preloaded with its own address. then, the contents of each
1059          ;Ac is checked for its address. if any ac does not contain
1060          ;Its address, this test fails.
1061
1062          000505
1063          000013          SN=SN+1
1064          ZZ=ZZ-1
1065 030773 302 13 0 00 000013      CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1066          STOP^
1067 030774 254 04 0 00 030775      HALT      .+1          ;Test failed if program halts here
1068 030775 324 00 0 00 030776      JUMPA     .+1          ;To loop change this instruction^
1069                                     ;In case of failure, loop to 'c500' address
1070
1071          ;*****
1072
1073          ;This test verifies that all acs exist. first, each ac is
1074          ;Preloaded with its own address. then, the contents of each
1075          ;Ac is checked for its address. if any ac does not contain
1076          ;Its address, this test fails.
1077
1078          000506
1079          000012          SN=SN+1
1080          ZZ=ZZ-1
1081 030776 302 12 0 00 000012      CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1082          STOP^
1083 030777 254 04 0 00 031000      HALT      .+1          ;Test failed if program halts here
1084 031000 324 00 0 00 031001      JUMPA     .+1          ;To loop change this instruction^
1085                                     ;In case of failure, loop to 'c500' address
1086
    
```



```

1087 ;*****
1088
1089
1090 ;This test verifies that all acs exist. first, each ac is
1091 ;Preloaded with its own address. then, the contents of each
1092 ;Ac is checked for its address. if any ac does not contain
1093 ;Its address, this test fails.
1094
1095         000507
1096         000011
1097 031001 302 11 0 00 000011      SN=SN+1      ZZ=ZZ-1
1098                                     CAIE      ZZ,ZZ      ;Check that each ac contains its own address
1099                                     STOP^
1100 031002 254 04 0 00 031003      HALT      .+1      ;Test failed if program halts here
1101 031003 324 00 0 00 031004      JUMPA     .+1      ;To loop change this instruction^
1102                                     ;In case of failure, loop to 'c500' address
1103
1104 ;*****
1105
1106 ;This test verifies that all acs exist. first, each ac is
1107 ;Preloaded with its own address. then, the contents of each
1108 ;Ac is checked for its address. if any ac does not contain
1109 ;Its address, this test fails.
1110
1111         000510
1112         000010
1113 031004 302 10 0 00 000010      SN=SN+1      ZZ=ZZ-1
1114                                     CAIE      ZZ,ZZ      ;Check that each ac contains its own address
1115                                     STOP^
1116 031005 254 04 0 00 031006      HALT      .+1      ;Test failed if program halts here
1117 031006 324 00 0 00 031007      JUMPA     .+1      ;To loop change this instruction^
1118                                     ;In case of failure, loop to 'c500' address
1119
1120 ;*****
1121
1122 ;This test verifies that all acs exist. first, each ac is
1123 ;Preloaded with its own address. then, the contents of each
1124 ;Ac is checked for its address. if any ac does not contain
1125 ;Its address, this test fails.
1126
1127         000511
1128         000007
1129 031007 302 07 0 00 000007      SN=SN+1      ZZ=ZZ-1
1130                                     CAIE      ZZ,ZZ      ;Check that each ac contains its own address
1131                                     STOP^
1132 031010 254 04 0 00 031011      HALT      .+1      ;Test failed if program halts here
1133 031011 324 00 0 00 031012      JUMPA     .+1      ;To loop change this instruction^
1134                                     ;In case of failure, loop to 'c500' address
1135
1136 ;*****
1137
1138 ;This test verifies that all acs exist. first, each ac is
1139 ;Preloaded with its own address. then, the contents of each
1140 ;Ac is checked for its address. if any ac does not contain
1141 ;Its address, this test fails.

```

```

1142
1143          000512      SN=SN+1
1144          000006      ZZ=ZZ-1
1145 031012 302 06 0 00 000006      CAIE    ZZ,ZZ      ;Check that each ac contains its own address
1146          STOP^
1147 031013 254 04 0 00 031014      HALT    .+1      ;Test failed if program halts here
1148 031014 324 00 0 00 031015      JUMPA   .+1      ;To loop change this instruction^
1149                                     ;In case of failure, loop to 'c500' address
1150
1151          ;*****
1152
1153          ;This test verifies that all acs exist. first, each ac is
1154          ;Preloaded with its own address. then, the contents of each
1155          ;Ac is checked for its address. if any ac does not contain
1156          ;Its address, this test fails.
1157
1158          000513      SN=SN+1
1159          000005      ZZ=ZZ-1
1160 031015 302 05 0 00 000005      CAIE    ZZ,ZZ      ;Check that each ac contains its own address
1161          STOP^
1162 031016 254 04 0 00 031017      HALT    .+1      ;Test failed if program halts here
1163 031017 324 00 0 00 031020      JUMPA   .+1      ;To loop change this instruction^
1164                                     ;In case of failure, loop to 'c500' address
1165
1166          ;*****
1167
1168          ;This test verifies that all acs exist. first, each ac is
1169          ;Preloaded with its own address. then, the contents of each
1170          ;Ac is checked for its address. if any ac does not contain
1171          ;Its address, this test fails.
1172
1173          000514      SN=SN+1
1174          000004      ZZ=ZZ-1
1175 031020 302 04 0 00 000004      CAIE    ZZ,ZZ      ;Check that each ac contains its own address
1176          STOP^
1177 031021 254 04 0 00 031022      HALT    .+1      ;Test failed if program halts here
1178 031022 324 00 0 00 031023      JUMPA   .+1      ;To loop change this instruction^
1179                                     ;In case of failure, loop to 'c500' address
1180
1181          ;*****
1182
1183          ;This test verifies that all acs exist. first, each ac is
1184          ;Preloaded with its own address. then, the contents of each
1185          ;Ac is checked for its address. if any ac does not contain
1186          ;Its address, this test fails.
1187
1188          000515      SN=SN+1
1189          000003      ZZ=ZZ-1
1190 031023 302 03 0 00 000003      CAIE    ZZ,ZZ      ;Check that each ac contains its own address
1191          STOP^
1192 031024 254 04 0 00 031025      HALT    .+1      ;Test failed if program halts here
1193 031025 324 00 0 00 031026      JUMPA   .+1      ;To loop change this instruction^
1194
1195
1196
    
```

```
1197                                     ;In case of failure, loop to 'c500' address
1198
1199                                     ;*****
1200
1201
1202                                     ;This test verifies that all acs exist. first, each ac is
1203                                     ;Preloaded with its own address. then, the contents of each
1204                                     ;Ac is checked for its address. if any ac does not contain
1205                                     ;Its address, this test fails.
1206
1207                                     000516
1208                                     000002
1209 031026 302 02 0 00 000002          SN=SN+1      ZZ=ZZ-1
1210                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1211                                     STOP^
1212 031027 254 04 0 00 031030          HALT      .+1          ;Test failed if program halts here
1213 031030 324 00 0 00 031031          JUMPA     .+1          ;To loop change this instruction^
1214                                     ;In case of failure, loop to 'c500' address
1215
1216                                     ;*****
1217
1218                                     ;This test verifies that all acs exist. first, each ac is
1219                                     ;Preloaded with its own address. then, the contents of each
1220                                     ;Ac is checked for its address. if any ac does not contain
1221                                     ;Its address, this test fails.
1222
1223                                     000517
1224                                     000001
1225 031031 302 01 0 00 000001          SN=SN+1      ZZ=ZZ-1
1226                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1227 031032 254 04 0 00 031033          STOP^
1228 031033 324 00 0 00 031034          HALT      .+1          ;Test failed if program halts here
1229                                     JUMPA     .+1          ;To loop change this instruction^
1230                                     ;In case of failure, loop to 'c500' address
1231
1232                                     ;*****
1233
1234                                     ;This test verifies that all acs exist. first, each ac is
1235                                     ;Preloaded with its own address. then, the contents of each
1236                                     ;Ac is checked for its address. if any ac does not contain
1237                                     ;Its address, this test fails.
1238
1239                                     000520
1240                                     000000
1241 031034 302 00 0 00 000000          SN=SN+1      ZZ=ZZ-1
1242                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1243 031035 254 04 0 00 031036          STOP^
1244 031036 324 00 0 00 031037          HALT      .+1          ;Test failed if program halts here
1245                                     JUMPA     .+1          ;To loop change this instruction^
1246                                     ;In case of failure, loop to 'c500' address
1247
1248                                     ;*****
```


1249 000600 SN=600
1250 000000 ZZ=0
1251
1252 ;This test verifies that an address within the ac range may be accessed as
1253 ;Either an ac or a memory location and that either reference refers to the
1254 ;Same hardware. each ac is preloaded with its address. then the contents
1255 ;Of each ac is checked for its address. if any ac does not contain its
1256 ;Address, this test fails.
1257
1258 C600: REPEAT ^D15,
1259 < ZZ=ZZ+1
1260 MOVEI ZZ ;Preload each ac with its address
1261 MOVEM ZZ ;By referencing each ac as memory.>
1262 ZZ=ZZ+1
1263 000001
1264 031037 201 00 0 00 000001 MOVEI ZZ ;Preload each ac with its address
1265 031040 202 00 0 00 000001 MOVEM ZZ ;By referencing each ac as memory.
1266 000002 ZZ=ZZ+1
1267 031041 201 00 0 00 000002 MOVEI ZZ ;Preload each ac with its address
1268 031042 202 00 0 00 000002 MOVEM ZZ ;By referencing each ac as memory.
1269 000003 ZZ=ZZ+1
1270 031043 201 00 0 00 000003 MOVEI ZZ ;Preload each ac with its address
1271 031044 202 00 0 00 000003 MOVEM ZZ ;By referencing each ac as memory.
1272 000004 ZZ=ZZ+1
1273 031045 201 00 0 00 000004 MOVEI ZZ ;Preload each ac with its address
1274 031046 202 00 0 00 000004 MOVEM ZZ ;By referencing each ac as memory.
1275 000005 ZZ=ZZ+1
1276 031047 201 00 0 00 000005 MOVEI ZZ ;Preload each ac with its address
1277 031050 202 00 0 00 000005 MOVEM ZZ ;By referencing each ac as memory.
1278 000006 ZZ=ZZ+1
1279 031051 201 00 0 00 000006 MOVEI ZZ ;Preload each ac with its address
1280 031052 202 00 0 00 000006 MOVEM ZZ ;By referencing each ac as memory.
1281 000007 ZZ=ZZ+1
1282 031053 201 00 0 00 000007 MOVEI ZZ ;Preload each ac with its address
1283 031054 202 00 0 00 000007 MOVEM ZZ ;By referencing each ac as memory.
1284 000010 ZZ=ZZ+1
1285 031055 201 00 0 00 000010 MOVEI ZZ ;Preload each ac with its address
1286 031056 202 00 0 00 000010 MOVEM ZZ ;By referencing each ac as memory.
1287 000011 ZZ=ZZ+1
1288 031057 201 00 0 00 000011 MOVEI ZZ ;Preload each ac with its address
1289 031060 202 00 0 00 000011 MOVEM ZZ ;By referencing each ac as memory.
1290 000012 ZZ=ZZ+1
1291 031061 201 00 0 00 000012 MOVEI ZZ ;Preload each ac with its address
1292 031062 202 00 0 00 000012 MOVEM ZZ ;By referencing each ac as memory.
1293 000013 ZZ=ZZ+1
1294 031063 201 00 0 00 000013 MOVEI ZZ ;Preload each ac with its address
1295 031064 202 00 0 00 000013 MOVEM ZZ ;By referencing each ac as memory.
1296 000014 ZZ=ZZ+1
1297 031065 201 00 0 00 000014 MOVEI ZZ ;Preload each ac with its address
1298 031066 202 00 0 00 000014 MOVEM ZZ ;By referencing each ac as memory.
1299 000015 ZZ=ZZ+1
1300 031067 201 00 0 00 000015 MOVEI ZZ ;Preload each ac with its address
1301 031070 202 00 0 00 000015 MOVEM ZZ ;By referencing each ac as memory.
1302 000016 ZZ=ZZ+1
1303 031071 201 00 0 00 000016 MOVEI ZZ ;Preload each ac with its address
1303 031072 202 00 0 00 000016 MOVEM ZZ ;By referencing each ac as memory.


```

1304          000017          ZZ=ZZ+1
1305 031073 201 00 0 00 000017      MOVEI  ZZ          ;Preload each ac with its address
1306 031074 202 00 0 00 000017      MOVEM  ZZ          ;By referencing each ac as memory.
1307
1308          000020          ZZ=20
1309
1310          REPEAT ^D15,<
1311 ;This test verifies that an address within the ac range may be accessed as
1312 ;Either an ac or a memory location and that either reference refers to the
1313 ;Same hardware. each ac is preloaded with its address. then the contents
1314 ;Of each ac is checked for its address. if any ac does not contain its
1315 ;Address, this test fails.
1316
1317 SN=SN+1
1318          ZZ=ZZ-1
1319          CAIE  ZZ,ZZ          ;Check that each ac contains its own address
1320          STOP
1321                                     ;In case of failure, loop to 'c600' address
1322
1323 ;*****
1324 >
1325
1326 ;This test verifies that an address within the ac range may be accessed as
1327 ;Either an ac or a memory location and that either reference refers to the
1328 ;Same hardware. each ac is preloaded with its address. then the contents
1329 ;Of each ac is checked for its address. if any ac does not contain its
1330 ;Address, this test fails.
1331
1332          000601
1333          000017
1334 031075 302 17 0 00 000017      CAIE  ZZ,ZZ          ;Check that each ac contains its own address
1335          STOP^
1336 031076 254 04 0 00 031077      HALT  .+1          ;Test failed if program halts here
1337 031077 324 00 0 00 031100      JUMPA .+1          ;To loop change this instruction^
1338                                     ;In case of failure, loop to 'c600' address
1339
1340 ;*****
1341
1342 ;This test verifies that an address within the ac range may be accessed as
1343 ;Either an ac or a memory location and that either reference refers to the
1344 ;Same hardware. each ac is preloaded with its address. then the contents
1345 ;Of each ac is checked for its address. if any ac does not contain its
1346 ;Address, this test fails.
1347
1348          000602
1349          000016
1350 031100 302 16 0 00 000016      CAIE  ZZ,ZZ          ;Check that each ac contains its own address
1351          STOP^
1352 031101 254 04 0 00 031102      HALT  .+1          ;Test failed if program halts here
1353 031102 324 00 0 00 031103      JUMPA .+1          ;To loop change this instruction^
1354                                     ;In case of failure, loop to 'c600' address
1355
1356 ;*****
1357
1358

```

```
1359
1360 ;This test verifies that an address within the ac range may be accessed as
1361 ;Either an ac or a memory location and that either reference refers to the
1362 ;Same hardware. each ac is preloaded with its address. then the contents
1363 ;Of each ac is checked for its address. if any ac does not contain its
1364 ;Address, this test fails.
1365
1366          000603
1367          000015
1368 031103 302 15 0 00 000015          SN=SN+1          ZZ=ZZ-1
1369                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1370                                     STOP^
1371 031104 254 04 0 00 031105          HALT      .+1          ;Test failed if program halts here
1372 031105 324 00 0 00 031106          JUMPA     .+1          ;To loop change this instruction^
1373                                     ;In case of failure, loop to 'c600' address
1374
1375 ;*****
1376
1377 ;This test verifies that an address within the ac range may be accessed as
1378 ;Either an ac or a memory location and that either reference refers to the
1379 ;Same hardware. each ac is preloaded with its address. then the contents
1380 ;Of each ac is checked for its address. if any ac does not contain its
1381 ;Address, this test fails.
1382
1383          000604
1384          000014
1385 031106 302 14 0 00 000014          SN=SN+1          ZZ=ZZ-1
1386                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1387                                     STOP^
1388 031107 254 04 0 00 031110          HALT      .+1          ;Test failed if program halts here
1389 031110 324 00 0 00 031111          JUMPA     .+1          ;To loop change this instruction^
1390                                     ;In case of failure, loop to 'c600' address
1391
1392 ;*****
1393
1394 ;This test verifies that an address within the ac range may be accessed as
1395 ;Either an ac or a memory location and that either reference refers to the
1396 ;Same hardware. each ac is preloaded with its address. then the contents
1397 ;Of each ac is checked for its address. if any ac does not contain its
1398 ;Address, this test fails.
1399
1400          000605
1401          000013
1402 031111 302 13 0 00 000013          SN=SN+1          ZZ=ZZ-1
1403                                     CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1404                                     STOP^
1405 031112 254 04 0 00 031113          HALT      .+1          ;Test failed if program halts here
1406 031113 324 00 0 00 031114          JUMPA     .+1          ;To loop change this instruction^
1407                                     ;In case of failure, loop to 'c600' address
1408
1409 ;*****
1410
1411 ;This test verifies that an address within the ac range may be accessed as
1412 ;Either an ac or a memory location and that either reference refers to the
1413 ;Same hardware. each ac is preloaded with its address. then the contents
```

```

1414 ;Of each ac is checked for its address. if any ac does not contain its
1415 ;Address, this test fails.
1416
1417 000606
1418 000012 SN=SN+1 ZZ=ZZ-1
1419 031114 302 12 0 00 000012 CAIE ZZ,ZZ ;Check that each ac contains its own address
1420 STOP^
1421 031115 254 04 0 00 031116 HALT .+1 ;Test failed if program halts here
1422 031116 324 00 0 00 031117 JUMPA .+1 ;To loop change this instruction^
1423 ;In case of failure, loop to "c600" address
1424
1425 ;*****
1426
1427
1428 ;This test verifies that an address within the ac range may be accessed as
1429 ;Either an ac or a memory location and that either reference refers to the
1430 ;Same hardware. each ac is preloaded with its address. then the contents
1431 ;Of each ac is checked for its address. if any ac does not contain its
1432 ;Address, this test fails.
1433
1434 000607
1435 000011 SN=SN+1 ZZ=ZZ-1
1436 031117 302 11 0 00 000011 CAIE ZZ,ZZ ;Check that each ac contains its own address
1437 STOP^
1438 031120 254 04 0 00 031121 HALT .+1 ;Test failed if program halts here
1439 031121 324 00 0 00 031122 JUMPA .+1 ;To loop change this instruction^
1440 ;In case of failure, loop to "c600" address
1441
1442 ;*****
1443
1444
1445 ;This test verifies that an address within the ac range may be accessed as
1446 ;Either an ac or a memory location and that either reference refers to the
1447 ;Same hardware. each ac is preloaded with its address. then the contents
1448 ;Of each ac is checked for its address. if any ac does not contain its
1449 ;Address, this test fails.
1450
1451 000610
1452 000010 SN=SN+1 ZZ=ZZ-1
1453 031122 302 10 0 00 000010 CAIE ZZ,ZZ ;Check that each ac contains its own address
1454 STOP^
1455 031123 254 04 0 00 031124 HALT .+1 ;Test failed if program halts here
1456 031124 324 00 0 00 031125 JUMPA .+1 ;To loop change this instruction^
1457 ;In case of failure, loop to "c600" address
1458
1459 ;*****
1460
1461
1462 ;This test verifies that an address within the ac range may be accessed as
1463 ;Either an ac or a memory location and that either reference refers to the
1464 ;Same hardware. each ac is preloaded with its address. then the contents
1465 ;Of each ac is checked for its address. if any ac does not contain its
1466 ;Address, this test fails.
1467
1468 000611 SN=SN+1
    
```



```

1469                                000007                ZZ=ZZ-1
1470 031125 302 07 0 00 000007        CAIE      ZZ,ZZ                ;Check that each ac contains its own address
1471                                STOP^
1472 031126 254 04 0 00 031127        HALT      .+1                ;Test failed if program halts here
1473 031127 324 00 0 00 031130        JUMPA     .+1                ;To loop change this instruction^
1474                                ;In case of failure, loop to 'c600' address
1475
1476                                ;*****
1477
1478
1479                                ;This test verifies that an address within the ac range may be accessed as
1480                                ;Either an ac or a memory location and that either reference refers to the
1481                                ;Same hardware.  each ac is preloaded with its address.  then the contents
1482                                ;Of each ac is checked for its address.  if any ac does not contain its
1483                                ;Address, this test fails.
1484
1485                                000612
1486                                000006                SN=SN+1
1487 031130 302 06 0 00 000006        ZZ=ZZ-1
1488                                CAIE      ZZ,ZZ                ;Check that each ac contains its own address
1489                                STOP^
1490 031131 254 04 0 00 031132        HALT      .+1                ;Test failed if program halts here
1491 031132 324 00 0 00 031133        JUMPA     .+1                ;To loop change this instruction^
1492                                ;In case of failure, loop to 'c600' address
1493
1494                                ;*****
1495
1496
1497                                ;This test verifies that an address within the ac range may be accessed as
1498                                ;Either an ac or a memory location and that either reference refers to the
1499                                ;Same hardware.  each ac is preloaded with its address.  then the contents
1500                                ;Of each ac is checked for its address.  if any ac does not contain its
1501                                ;Address, this test fails.
1502
1503                                000613
1504                                000005                SN=SN+1
1505 031133 302 05 0 00 000005        ZZ=ZZ-1
1506                                CAIE      ZZ,ZZ                ;Check that each ac contains its own address
1507 031134 254 04 0 00 031135        HALT      .+1                ;Test failed if program halts here
1508 031135 324 00 0 00 031136        JUMPA     .+1                ;To loop change this instruction^
1509                                ;In case of failure, loop to 'c600' address
1510
1511                                ;*****
1512
1513
1514                                ;This test verifies that an address within the ac range may be accessed as
1515                                ;Either an ac or a memory location and that either reference refers to the
1516                                ;Same hardware.  each ac is preloaded with its address.  then the contents
1517                                ;Of each ac is checked for its address.  if any ac does not contain its
1518                                ;Address, this test fails.
1519
1520                                000614
1521                                000004                SN=SN+1
1522 031136 302 04 0 00 000004        ZZ=ZZ-1
1523 031137 254 04 0 00 031140        CAIE      ZZ,ZZ                ;Check that each ac contains its own address
                                STOP^
                                HALT      .+1                ;Test failed if program halts here

```



```

1524 031140 324 00 0 00 031141          JUMPA      .+1          ;To loop change this instruction^
1525                                         ;In case of failure, loop to 'c600' address
1526
1527 ;*****
1528
1529
1530 ;This test verifies that an address within the ac range may be accessed as
1531 ;Either an ac or a memory location and that either reference refers to the
1532 ;Same hardware. each ac is preloaded with its address. then the contents
1533 ;Of each ac is checked for its address. if any ac does not contain its
1534 ;Address, this test fails.
1535
1536             000615
1537             000003          SN=SN+1
1538 031141 302 03 0 00 000003          ZZ=ZZ-1
1539                                         CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1540                                         STOP^
1541 031142 254 04 0 00 031143          HALT      .+1          ;Test failed if program halts here
1542 031143 324 00 0 00 031144          JUMPA      .+1          ;To loop change this instruction^
1543                                         ;In case of failure, loop to 'c600' address
1544
1545 ;*****
1546
1547 ;This test verifies that an address within the ac range may be accessed as
1548 ;Either an ac or a memory location and that either reference refers to the
1549 ;Same hardware. each ac is preloaded with its address. then the contents
1550 ;Of each ac is checked for its address. if any ac does not contain its
1551 ;Address, this test fails.
1552
1553             000616
1554             000002          SN=SN+1
1555 031144 302 02 0 00 000002          ZZ=ZZ-1
1556                                         CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1557                                         STOP^
1558 031145 254 04 0 00 031146          HALT      .+1          ;Test failed if program halts here
1559 031146 324 00 0 00 031147          JUMPA      .+1          ;To loop change this instruction^
1560                                         ;In case of failure, loop to 'c600' address
1561
1562 ;*****
1563
1564 ;This test verifies that an address within the ac range may be accessed as
1565 ;Either an ac or a memory location and that either reference refers to the
1566 ;Same hardware. each ac is preloaded with its address. then the contents
1567 ;Of each ac is checked for its address. if any ac does not contain its
1568 ;Address, this test fails.
1569
1570             000617
1571             000001          SN=SN+1
1572 031147 302 01 0 00 000001          ZZ=ZZ-1
1573                                         CAIE      ZZ,ZZ          ;Check that each ac contains its own address
1574                                         STOP^
1575 031150 254 04 0 00 031151          HALT      .+1          ;Test failed if program halts here
1576 031151 324 00 0 00 031152          JUMPA      .+1          ;To loop change this instruction^
1577                                         ;In case of failure, loop to 'c600' address
1578
1579 ;*****

```

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DFKAD1 MAC 1-Oct-84 16:01 TEST OF AC HARDWARE AND INDEX REGISTERS

SEQ 0042

1579

```

1580          000700      SN=700
1581          000000      ZZ=0
1582
1583      C700: REPEAT ^D15,<
1584      ;This test verifies that the index registers are accessible. first, an
1585      ;Index register is preloaded with its address. then, it is referenced
1586      ;As an index register. if it contains its address, this test passes.
1587      ;This test is repeated 15 times in order to test each index register.
1588
1589      SN=SN+1
1590          ZZ=ZZ+1
1591          MOVEI    ZZ,ZZ      ;Preload index register with its address
1592          CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1593          STOP
1594
1595      ;*****
1596      >
1597
1598      ;This test verifies that the index registers are accessible. first, an
1599      ;Index register is preloaded with its address. then, it is referenced
1600      ;As an index register. if it contains its address, this test passes.
1601      ;This test is repeated 15 times in order to test each index register.
1602
1603          000701
1604          000001
1605      031152  201 01 0 00 000001
1606      031153  302 01 0 01 000000
1607
1608      031154  254 04 0 00 031155
1609      031155  324 00 0 00 031156
1610
1611          ZZ=ZZ+1
1612          MOVEI    ZZ,ZZ      ;Preload index register with its address
1613          CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1614          STOP^
1615          HALT     .+1        ;Test failed if program halts here
1616          JUMPA    .+1        ;To loop change this instruction^
1617
1618      ;*****
1619
1620      ;This test verifies that the index registers are accessible. first, an
1621      ;Index register is preloaded with its address. then, it is referenced
1622      ;As an index register. if it contains its address, this test passes.
1623      ;This test is repeated 15 times in order to test each index register.
1624
1625          000702
1626          000002
1627      031156  201 02 0 00 000002
1628      031157  302 02 0 02 000000
1629
1630      031160  254 04 0 00 031161
1631      031161  324 00 0 00 031162
1632
1633          ZZ=ZZ+1
1634          MOVEI    ZZ,ZZ      ;Preload index register with its address
1635          CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1636          STOP^
1637          HALT     .+1        ;Test failed if program halts here
1638          JUMPA    .+1        ;To loop change this instruction^
1639
1640      ;*****
1641
1642      ;This test verifies that the index registers are accessible. first, an
1643      ;Index register is preloaded with its address. then, it is referenced
1644      ;As an index register. if it contains its address, this test passes.
1645      ;This test is repeated 15 times in order to test each index register.
  
```

```

1635          000703      SN=SN+1
1636          000003      ZZ=ZZ+1
1637 031162 201 03 0 00 000003      MOVEI    ZZ,ZZ      ;Preload index register with its address
1638 031163 302 03 0 03 000000      CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1639          STOP^
1640 031164 254 04 0 00 031165      HALT     .+1      ;Test failed if program halts here
1641 031165 324 00 0 00 031166      JUMPA    .+1      ;To loop change this instruction^
1642
1643          ;*****
1644
1645          ;This test verifies that the index registers are accessible. first, an
1646          ;Index register is preloaded with its address. then, it is referenced
1647          ;As an index register. if it contains its address, this test passes.
1648          ;This test is repeated 15 times in order to test each index register.
1649
1650          000704      SN=SN+1
1651          000004      ZZ=ZZ+1
1652          000004      MOVEI    ZZ,ZZ      ;Preload index register with its address
1653 031166 201 04 0 00 000004      CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1654 031167 302 04 0 04 000000      STOP^
1655          HALT     .+1      ;Test failed if program halts here
1656 031170 254 04 0 00 031171      JUMPA    .+1      ;To loop change this instruction^
1657 031171 324 00 0 00 031172
1658
1659          ;*****
1660
1661          ;This test verifies that the index registers are accessible. first, an
1662          ;Index register is preloaded with its address. then, it is referenced
1663          ;As an index register. if it contains its address, this test passes.
1664          ;This test is repeated 15 times in order to test each index register.
1665
1666          000705      SN=SN+1
1667          000005      ZZ=ZZ+1
1668          000005      MOVEI    ZZ,ZZ      ;Preload index register with its address
1669 031172 201 05 0 00 000005      CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1670 031173 302 05 0 05 000000      STOP^
1671          HALT     .+1      ;Test failed if program halts here
1672 031174 254 04 0 00 031175      JUMPA    .+1      ;To loop change this instruction^
1673 031175 324 00 0 00 031176
1674
1675          ;*****
1676
1677          ;This test verifies that the index registers are accessible. first, an
1678          ;Index register is preloaded with its address. then, it is referenced
1679          ;As an index register. if it contains its address, this test passes.
1680          ;This test is repeated 15 times in order to test each index register.
1681
1682          000706      SN=SN+1
1683          000006      ZZ=ZZ+1
1684          000006      MOVEI    ZZ,ZZ      ;Preload index register with its address
1685 031176 201 06 0 00 000006      CAIE     ZZ,(ZZ)    ;Pass if index register contains its address
1686 031177 302 06 0 06 000000      STOP^
1687          HALT     .+1      ;Test failed if program halts here
1688 031200 254 04 0 00 031201      JUMPA    .+1      ;To loop change this instruction^
1689 031201 324 00 0 00 031202
    
```



```

1690
1691 ;*****
1692
1693
1694 ;This test verifies that the index registers are accessible. first, an
1695 ;Index register is preloaded with its address. then, it is referenced
1696 ;As an index register. if it contains its address, this test passes.
1697 ;This test is repeated 15 times in order to test each index register.
1698
1699         000707
1700         000007
1701 031202 201 07 0 00 000007      ZZ=ZZ+1
1702 031203 302 07 0 07 000000      MOVEI  ZZ,ZZ      ;Preload index register with its address
1703                                     CAIE   ZZ,(ZZ)      ;Pass if index register contains its address
1704                                     STOP^
1705 031204 254 04 0 00 031205      HALT    .+1          ;Test failed if program halts here
1706 031205 324 00 0 00 031206      JUMPA   .+1          ;To loop change this instruction^
1707
1708 ;*****
1709
1710 ;This test verifies that the index registers are accessible. first, an
1711 ;Index register is preloaded with its address. then, it is referenced
1712 ;As an index register. if it contains its address, this test passes.
1713 ;This test is repeated 15 times in order to test each index register.
1714
1715         000710
1716         000010
1717 031206 201 10 0 00 000010      ZZ=ZZ+1
1718 031207 302 10 0 10 000000      MOVEI  ZZ,ZZ      ;Preload index register with its address
1719                                     CAIE   ZZ,(ZZ)      ;Pass if index register contains its address
1720                                     STOP^
1721 031210 254 04 0 00 031211      HALT    .+1          ;Test failed if program halts here
1722 031211 324 00 0 00 031212      JUMPA   .+1          ;To loop change this instruction^
1723
1724 ;*****
1725
1726 ;This test verifies that the index registers are accessible. first, an
1727 ;Index register is preloaded with its address. then, it is referenced
1728 ;As an index register. if it contains its address, this test passes.
1729 ;This test is repeated 15 times in order to test each index register.
1730
1731         000711
1732         000011
1733 031212 201 11 0 00 000011      ZZ=ZZ+1
1734 031213 302 11 0 11 000000      MOVEI  ZZ,ZZ      ;Preload index register with its address
1735                                     CAIE   ZZ,(ZZ)      ;Pass if index register contains its address
1736                                     STOP^
1737 031214 254 04 0 00 031215      HALT    .+1          ;Test failed if program halts here
1738 031215 324 00 0 00 031216      JUMPA   .+1          ;To loop change this instruction^
1739
1740 ;*****
1741
1742 ;This test verifies that the index registers are accessible. first, an
1743 ;Index register is preloaded with its address. then, it is referenced
1744 ;As an index register. if it contains its address, this test passes.
    
```

```

1745 ;This test is repeated 15 times in order to test each index register.
1746
1747         000712
1748         000012
1749 031216 201 12 0 00 000012
1750 031217 302 12 0 12 000000
1751
1752 031220 254 04 0 00 031221
1753 031221 324 00 0 00 031222
1754
1755
1756
1757
1758 ;*****
1759 ;This test verifies that the index registers are accessible. first, an
1760 ;Index register is preloaded with its address. then, it is referenced
1761 ;As an index register. if it contains its address, this test passes.
1762 ;This test is repeated 15 times in order to test each index register.
1763
1764         000713
1765         000013
1766 031222 201 13 0 00 000013
1767 031223 302 13 0 13 000000
1768
1769 031224 254 04 0 00 031225
1770 031225 324 00 0 00 031226
1771
1772
1773
1774 ;*****
1775 ;This test verifies that the index registers are accessible. first, an
1776 ;Index register is preloaded with its address. then, it is referenced
1777 ;As an index register. if it contains its address, this test passes.
1778 ;This test is repeated 15 times in order to test each index register.
1779
1780         000714
1781         000014
1782 031226 201 14 0 00 000014
1783 031227 302 14 0 14 000000
1784
1785 031230 254 04 0 00 031231
1786 031231 324 00 0 00 031232
1787
1788
1789
1790 ;*****
1791 ;This test verifies that the index registers are accessible. first, an
1792 ;Index register is preloaded with its address. then, it is referenced
1793 ;As an index register. if it contains its address, this test passes.
1794 ;This test is repeated 15 times in order to test each index register.
1795
1796         000715
1797         000015
1798 031232 201 15 0 00 000015
1799 031233 302 15 0 15 000000

```

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

CAIE ZZ,(ZZ)

STOP^

HALT .+1

JUMPA .+1

;Preload index register with its address

;Pass if index register contains its address

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that the index registers are accessible. first, an
 ;Index register is preloaded with its address. then, it is referenced
 ;As an index register. if it contains its address, this test passes.
 ;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

CAIE ZZ,(ZZ)

STOP^

HALT .+1

JUMPA .+1

;Preload index register with its address

;Pass if index register contains its address

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that the index registers are accessible. first, an
 ;Index register is preloaded with its address. then, it is referenced
 ;As an index register. if it contains its address, this test passes.
 ;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

CAIE ZZ,(ZZ)

STOP^

HALT .+1

JUMPA .+1

;Preload index register with its address

;Pass if index register contains its address

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that the index registers are accessible. first, an
 ;Index register is preloaded with its address. then, it is referenced
 ;As an index register. if it contains its address, this test passes.
 ;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

CAIE ZZ,(ZZ)

STOP^

;Preload index register with its address

;Pass if index register contains its address

```

1800 031234 254 04 0 00 031235          HALT      .+1          ;Test failed if program halts here
1801 031235 324 00 0 00 031236          JUMPA     .+1          ;To loop change this instruction^
1802
1803 ;*****
1804
1805
1806 ;This test verifies that the index registers are accessable. first, an
1807 ;Index register is preloaded with its address. then, it is referenced
1808 ;As an index register. if it contains its address, this test passes.
1809 ;This test is repeated 15 times in order to test each index register.
1810
1811                                000716
1812                                000016
1813 031236 201 16 0 00 000016          ZZ=ZZ+1
1814 031237 302 16 0 16 000000          MOVEI     ZZ,ZZ          ;Preload index register with its address
1815                                CAIE      ZZ,(ZZ)          ;Pass if index register contains its address
1816                                STOP^
1816 031240 254 04 0 00 031241          HALT      .+1          ;Test failed if program halts here
1817 031241 324 00 0 00 031242          JUMPA     .+1          ;To loop change this instruction^
1818
1819 ;*****
1820
1821
1822 ;This test verifies that the index registers are accessable. first, an
1823 ;Index register is preloaded with its address. then, it is referenced
1824 ;As an index register. if it contains its address, this test passes.
1825 ;This test is repeated 15 times in order to test each index register.
1826
1827                                000717
1828                                000017
1829 031242 201 17 0 00 000017          ZZ=ZZ+1
1830 031243 302 17 0 17 000000          MOVEI     ZZ,ZZ          ;Preload index register with its address
1831                                CAIE      ZZ,(ZZ)          ;Pass if index register contains its address
1832                                STOP^
1832 031244 254 04 0 00 031245          HALT      .+1          ;Test failed if program halts here
1833 031245 324 00 0 00 031246          JUMPA     .+1          ;To loop change this instruction^
1834
1835 ;*****
1836
    
```



```

1837          001000          SN=1000
1838          000000          ZZ=0
1839
1840          C1000: REPEAT ^D15,<
1841          ;This test verifies that all index registers index correctly. first, both
1842          ;Halves of the index register are preloaded with its address. then, the
1843          ;Index register is referenced. it is then checked for its address in both
1844          ;Halves. if it contains its address in both halves this test passes.
1845          ;This test is repeated 15 times in order to test each index register.
1846
1847          SN=SN+1
1848          ZZ=ZZ+1
1849          MOVEI    ZZ,ZZ          ;Preload both halves of index reg with its address
1850          HRLI     ZZ,ZZ          ;Pass if index register contains its address
1851          CAME     ZZ,(ZZ)        ;In both halves
1852          STOP
1853
1854          ;*****
1855          >
1856
1857          ;This test verifies that all index registers index correctly. first, both
1858          ;Halves of the index register are preloaded with its address. then, the
1859          ;Index register is referenced. it is then checked for its address in both
1860          ;Halves. if it contains its address in both halves this test passes.
1861          ;This test is repeated 15 times in order to test each index register.
1862
1863          001001
1864          000001
1865          031246 201 01 0 00 000001
1866          031247 505 01 0 00 000001
1867          031250 312 01 0 01 000000
1868
1869          031251 254 04 0 00 031252
1870          031252 324 00 0 00 031253
1871
1872          SN=SN+1
1873          ZZ=ZZ+1
1874          MOVEI    ZZ,ZZ          ;Preload both halves of index reg with its address
1875          HRLI     ZZ,ZZ          ;Pass if index register contains its address
1876          CAME     ZZ,(ZZ)        ;In both halves
1877          STOP^
1878          HALT     .+1            ;Test failed if program halts here
1879          JUMPA    .+1            ;To loop change this instruction^
1880
1881          ;*****
1882
1883          ;This test verifies that all index registers index correctly. first, both
1884          ;Halves of the index register are preloaded with its address. then, the
1885          ;Index register is referenced. it is then checked for its address in both
1886          ;Halves. if it contains its address in both halves this test passes.
1887          ;This test is repeated 15 times in order to test each index register.
1888
1889          001002
1890          000002
1891          031253 201 02 0 00 000002
1892          031254 505 02 0 00 000002
1893          031255 312 02 0 02 000000
1894
1895          031256 254 04 0 00 031257
1896          031257 324 00 0 00 031260
1897
1898          SN=SN+1
1899          ZZ=ZZ+1
1900          MOVEI    ZZ,ZZ          ;Preload both halves of index reg with its address
1901          HRLI     ZZ,ZZ          ;Pass if index register contains its address
1902          CAME     ZZ,(ZZ)        ;In both halves
1903          STOP^
1904          HALT     .+1            ;Test failed if program halts here
1905          JUMPA    .+1            ;To loop change this instruction^
1906
1907          ;*****
  
```



```

1892
1893 ;This test verifies that all index registers index correctly. first, both
1894 ;Halves of the index register are preloaded with its address. then, the
1895 ;Index register is referenced. it is then checked for its address in both
1896 ;Halves. if it contains its address in both halves this test passes.
1897 ;This test is repeated 15 times in order to test each index register.
1898
1899         001003
1900         000003
1901 031260 201 03 0 00 000003      SN=SN+1      ZZ=ZZ+1
1902 031261 505 03 0 00 000003      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1903 031262 312 03 0 03 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1904                                CAME      ZZ,(ZZ)      ;In both halves
1905                                STOP^
1906 031263 254 04 0 00 031264      HALT      .+1      ;Test failed if program halts here
1907 031264 324 00 0 00 031265      JUMPA     .+1      ;To loop change this instruction^
1908
1909 ;*****
1910
1911 ;This test verifies that all index registers index correctly. first, both
1912 ;Halves of the index register are preloaded with its address. then, the
1913 ;Index register is referenced. it is then checked for its address in both
1914 ;Halves. if it contains its address in both halves this test passes.
1915 ;This test is repeated 15 times in order to test each index register.
1916
1917         001004
1918         000004
1919 031265 201 04 0 00 000004      SN=SN+1      ZZ=ZZ+1
1920 031266 505 04 0 00 000004      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1921 031267 312 04 0 04 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1922                                CAME      ZZ,(ZZ)      ;In both halves
1923                                STOP^
1924 031270 254 04 0 00 031271      HALT      .+1      ;Test failed if program halts here
1925 031271 324 00 0 00 031272      JUMPA     .+1      ;To loop change this instruction^
1926
1927 ;*****
1928
1929 ;This test verifies that all index registers index correctly. first, both
1930 ;Halves of the index register are preloaded with its address. then, the
1931 ;Index register is referenced. it is then checked for its address in both
1932 ;Halves. if it contains its address in both halves this test passes.
1933 ;This test is repeated 15 times in order to test each index register.
1934
1935         001005
1936         000005
1937 031272 201 05 0 00 000005      SN=SN+1      ZZ=ZZ+1
1938 031273 505 05 0 00 000005      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1939 031274 312 05 0 05 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1940                                CAME      ZZ,(ZZ)      ;In both halves
1941                                STOP^
1942 031275 254 04 0 00 031276      HALT      .+1      ;Test failed if program halts here
1943 031276 324 00 0 00 031277      JUMPA     .+1      ;To loop change this instruction^
1944
1945 ;*****
1946

```

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1947 ;This test verifies that all index registers index correctly. first, both
1948 ;Halves of the index register are preloaded with its address. then, the
1949 ;Index register is referenced. it is then checked for its address in both
1950 ;Halves. if it contains its address in both halves this test passes.
1951 ;This test is repeated 15 times in order to test each index register.
1952
1953         001006
1954         000006
1955 031277 201 06 0 00 000006      SN=SN+1      ZZ=ZZ+1
1956 031300 505 06 0 00 000006      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1957 031301 312 06 0 06 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1958                                CAME      ZZ,(ZZ)      ;In both halves
1959                                STOP^
1959 031302 254 04 0 00 031303      HALT      .+1      ;Test failed if program halts here
1960 031303 324 00 0 00 031304      JUMPA     .+1      ;To loop change this instruction^
1961
1962 ;*****
1963
1964 ;This test verifies that all index registers index correctly. first, both
1965 ;Halves of the index register are preloaded with its address. then, the
1966 ;Index register is referenced. it is then checked for its address in both
1967 ;Halves. if it contains its address in both halves this test passes.
1968 ;This test is repeated 15 times in order to test each index register.
1969
1970
1971         001007
1972         000007
1973 031304 201 07 0 00 000007      SN=SN+1      ZZ=ZZ+1
1974 031305 505 07 0 00 000007      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1975 031306 312 07 0 07 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1976                                CAME      ZZ,(ZZ)      ;In both halves
1977                                STOP^
1977 031307 254 04 0 00 031310      HALT      .+1      ;Test failed if program halts here
1978 031310 324 00 0 00 031311      JUMPA     .+1      ;To loop change this instruction^
1979
1980 ;*****
1981
1982 ;This test verifies that all index registers index correctly. first, both
1983 ;Halves of the index register are preloaded with its address. then, the
1984 ;Index register is referenced. it is then checked for its address in both
1985 ;Halves. if it contains its address in both halves this test passes.
1986 ;This test is repeated 15 times in order to test each index register.
1987
1988
1989         001010
1990         000010
1991 031311 201 10 0 00 000010      SN=SN+1      ZZ=ZZ+1
1992 031312 505 10 0 00 000010      MOVEI      ZZ,ZZ      ;Preload both halves of index reg with its address
1993 031313 312 10 0 10 000000      HRLI      ZZ,ZZ      ;Pass if index register contains its address
1994                                CAME      ZZ,(ZZ)      ;In both halves
1995                                STOP^
1995 031314 254 04 0 00 031315      HALT      .+1      ;Test failed if program halts here
1996 031315 324 00 0 00 031316      JUMPA     .+1      ;To loop change this instruction^
1997
1998 ;*****
1999
2000 ;This test verifies that all index registers index correctly. first, both
2001

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;Halves of the index register are preloaded with its address. then, the
;Index register is referenced. it is then checked for its address in both
;Halves. if it contains its address in both halves this test passes.
;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

;Preload both halves of index reg with its address

HRLI ZZ,ZZ

;Pass if index register contains its address

CAME ZZ,(ZZ)

;In both halves

STOP^

HALT .+1

;Test failed if program halts here

JUMPA .+1

;To loop change this instruction^

;*****

;This test verifies that all index registers index correctly. first, both
;Halves of the index register are preloaded with its address. then, the
;Index register is referenced. it is then checked for its address in both
;Halves. if it contains its address in both halves this test passes.
;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

;Preload both halves of index reg with its address

HRLI ZZ,ZZ

;Pass if index register contains its address

CAME ZZ,(ZZ)

;In both halves

STOP^

HALT .+1

;Test failed if program halts here

JUMPA .+1

;To loop change this instruction^

;*****

;This test verifies that all index registers index correctly. first, both
;Halves of the index register are preloaded with its address. then, the
;Index register is referenced. it is then checked for its address in both
;Halves. if it contains its address in both halves this test passes.
;This test is repeated 15 times in order to test each index register.

SN=SN+1

ZZ=ZZ+1

MOVEI ZZ,ZZ

;Preload both halves of index reg with its address

HRLI ZZ,ZZ

;Pass if index register contains its address

CAME ZZ,(ZZ)

;In both halves

STOP^

HALT .+1

;Test failed if program halts here

JUMPA .+1

;To loop change this instruction^

;*****

;This test verifies that all index registers index correctly. first, both
;Halves of the index register are preloaded with its address. then, the


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2057 ;Index register is referenced. it is then checked for its address in both
2058 ;Halves. if it contains its address in both halves this test passes.
2059 ;This test is repeated 15 times in order to test each index register.
2060
2061         001014
2062         000014
2063 031335 201 14 0 00 000014
2064 031336 505 14 0 00 000014
2065 031337 312 14 0 14 000000
2066
2067 031340 254 04 0 00 031341
2068 031341 324 00 0 00 031342
2069
2070 ;*****
2071
2072 ;This test verifies that all index registers index correctly. first, both
2073 ;Halves of the index register are preloaded with its address. then, the
2074 ;Index register is referenced. it is then checked for its address in both
2075 ;Halves. if it contains its address in both halves this test passes.
2076 ;This test is repeated 15 times in order to test each index register.
2077
2078         001015
2079         000015
2080
2081 031342 201 15 0 00 000015
2082 031343 505 15 0 00 000015
2083 031344 312 15 0 15 000000
2084
2085 031345 254 04 0 00 031346
2086 031346 324 00 0 00 031347
2087
2088 ;*****
2089
2090 ;This test verifies that all index registers index correctly. first, both
2091 ;Halves of the index register are preloaded with its address. then, the
2092 ;Index register is referenced. it is then checked for its address in both
2093 ;Halves. if it contains its address in both halves this test passes.
2094 ;This test is repeated 15 times in order to test each index register.
2095
2096         001016
2097         000016
2098
2099 031347 201 16 0 00 000016
2100 031350 505 16 0 00 000016
2101 031351 312 16 0 16 000000
2102
2103 031352 254 04 0 00 031353
2104 031353 324 00 0 00 031354
2105
2106 ;*****
2107
2108 ;This test verifies that all index registers index correctly. first, both
2109 ;Halves of the index register are preloaded with its address. then, the
2110 ;Index register is referenced. it is then checked for its address in both
2111

```



```

2112 ;Halves. if it contains its address in both halves this test passes.
2113 ;This test is repeated 15 times in order to test each index register.
2114
2115 001017
2116 000017 SN=SN+1 ZZ=ZZ+1
2117 031354 201 17 0 00 000017 MOVEI ZZ,ZZ ;Preload both halves of index reg with its address
2118 031355 505 17 0 00 000017 HRLI ZZ,ZZ ;Pass if index register contains its address
2119 031356 312 17 0 17 000000 CAME ZZ,(ZZ) ;In both halves
2120 STOP^
2121 031357 254 04 0 00 031360 HALT .+1 ;Test failed if program halts here
2122 031360 324 00 0 00 031361 JUMPA .+1 ;To loop change this instruction^
2123
2124 ;*****
2125

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2166
2167
2168
2169
2170
2171
2172
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2180

031361 476 00 0 00 000003
 031362 402 00 0 00 000001
 031363 201 02 0 00 000001
 031364 200 03 0 02 000000
 031365 332 00 0 00 000003
 031366 254 04 0 00 031367
 031367 324 00 0 00 031370

001200
000000

001201
000000

SUBTTL TEST OF INDEX REGISTER ADDRESSING

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a 0, the final result in ac3 should be 0. if
 ;C(ac3)=0, this test passes.

C1100: SETOM 3 ;Preload ac3 with -1,,1
 SETZM 1 ;Preload ac1 with 0
 MOVEI 2,1 ;Setup index register 2 with 1
 MOVE 3,(2) ;*Fwt from indexed location
 SKIPE 3 ;Test indexing
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****

SN=1200
ZZ=0

C1200: REPEAT ^D18,<
 ;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1
 ZZ=ZZ+ZZ
 IFE ZZ,<ZZ=1>
 SETOM 3 ;Preload ac3 with -1,,-1
 MOVEI 1,ZZ ;Preload ac1 with floating 1
 MOVEI 2,1 ;Setup index register
 MOVE 3,(2) ;*Fwt from indexed location
 CAIE 3,ZZ ;Test indexing
 STOP

;*****
 >

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1
ZZ=ZZ+ZZ

```

2181                                000001                                IFE      ZZ,<ZZ=1>
2182 031370 476 00 0 00 000003      SETOM     3                                ;Preload ac3 with -1,-1
2183 031371 201 01 0 00 000001      MOVEI     1,ZZ                                ;Preload ac1 with floating 1
2184 031372 201 02 0 00 000001      MOVEI     2,1                                ;Setup index register
2185 031373 200 03 0 02 000000      MOVE      3,(2)                                ;*Fwt from indexed location
2186 031374 302 03 0 00 000001      CAIE      3,ZZ                                ;Test indexing
2187                                STOP^
2188 031375 254 04 0 00 031376      HALT      .+1                                ;Test failed if program halts here
2189 031376 324 00 0 00 031377      JUMPA     .+1                                ;To loop change this instruction^
2190
2191 ;*****
2192
2193
2194 ;This test verifies that index register addressing functions correctly.
2195 ;In this test, a move instruction using indexing is executed. the move
2196 ;Instruction should place the contents of the location specified by index
2197 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2198 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2199 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2200
2201                                001202
2202                                000002      SN=SN+1
2203                                ZZ=ZZ+ZZ
2204 031377 476 00 0 00 000003      IFE      ZZ,<ZZ=1>                                ;Preload ac3 with -1,-1
2205 031400 201 01 0 00 000002      SETOM     3                                ;Preload ac1 with floating 1
2206 031401 201 02 0 00 000001      MOVEI     1,ZZ                                ;Setup index register
2207 031402 200 03 0 02 000000      MOVEI     2,1                                ;*Fwt from indexed location
2208 031403 302 03 0 00 000002      MOVE      3,(2)                                ;Test indexing
2209                                CAIE      3,ZZ
2210                                STOP^
2211 031404 254 04 0 00 031405      HALT      .+1                                ;Test failed if program halts here
2212 031405 324 00 0 00 031406      JUMPA     .+1                                ;To loop change this instruction^
2213
2214 ;*****
2215
2216
2217 ;This test verifies that index register addressing functions correctly.
2218 ;In this test, a move instruction using indexing is executed. the move
2219 ;Instruction should place the contents of the location specified by index
2220 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2221 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2222 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2223
2224                                001203
2225                                000004      SN=SN+1
2226                                ZZ=ZZ+ZZ
2227 031406 476 00 0 00 000003      IFE      ZZ,<ZZ=1>                                ;Preload ac3 with -1,-1
2228 031407 201 01 0 00 000004      SETOM     3                                ;Preload ac1 with floating 1
2229 031410 201 02 0 00 000001      MOVEI     1,ZZ                                ;Setup index register
2230 031411 200 03 0 02 000000      MOVEI     2,1                                ;*Fwt from indexed location
2231 031412 302 03 0 00 000004      MOVE      3,(2)                                ;Test indexing
2232                                CAIE      3,ZZ
2233                                STOP^
2234 031413 254 04 0 00 031414      HALT      .+1                                ;Test failed if program halts here
2235 031414 324 00 0 00 031415      JUMPA     .+1                                ;To loop change this instruction^
2236
2237 ;*****

```

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001204
000010
031415 476 00 0 00 000003
031416 201 01 0 00 000010
031417 201 02 0 00 000001
031420 200 03 0 02 000000
031421 302 03 0 00 000010
031422 254 04 0 00 031423
031423 324 00 0 00 031424
001205
000020
031424 476 00 0 00 000003
031425 201 01 0 00 000020
031426 201 02 0 00 000001
031427 200 03 0 02 000000
031430 302 03 0 00 000020
031431 254 04 0 00 031432
031432 324 00 0 00 031433
001206
000040

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ

IFE ZZ,<ZZ=1>

SETOM 3

MOVEI 1,ZZ

MOVEI 2,1

MOVE 3,(2)

CAIE 3,ZZ

STOP^

HALT .+1

JUMPA .+1

;Preload ac3 with -1,-1

;Preload ac1 with floating 1

;Setup index register

;*Fwt from indexed location

;Test indexing

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ

IFE ZZ,<ZZ=1>

SETOM 3

MOVEI 1,ZZ

MOVEI 2,1

MOVE 3,(2)

CAIE 3,ZZ

STOP^

HALT .+1

JUMPA .+1

;Preload ac3 with -1,-1

;Preload ac1 with floating 1

;Setup index register

;*Fwt from indexed location

;Test indexing

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ


```

2291                                     IFE      ZZ,<ZZ=1>
2292 031433 476 00 0 00 000003      SETOM     3          ;Preload ac3 with -1,-1
2293 031434 201 01 0 00 000040      MOVEI     1,ZZ      ;Preload ac1 with floating 1
2294 031435 201 02 0 00 000001      MOVEI     2,1        ;Setup index register
2295 031436 200 03 0 02 000000      MOVE      3,(2)      ;*Fwt from indexed location
2296 031437 302 03 0 00 000040      CAIE      3,ZZ      ;Test indexing
2297                                     STOP^
2298 031440 254 04 0 00 031441      HALT      .+1        ;Test failed if program halts here
2299 031441 324 00 0 00 031442      JUMPA     .+1        ;To loop change this instruction^
2300
2301 ;*****
2302
2303 ;This test verifies that index register addressing functions correctly.
2304 ;In this test, a move instruction using indexing is executed. the move
2305 ;Instruction should place the contents of the location specified by index
2306 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2307 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2308 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2309
2310                                     001207
2311                                     000100      SN=SN+1
2312                                     ZZ=ZZ+ZZ
2313                                     IFE      ZZ,<ZZ=1>
2314 031442 476 00 0 00 000003      SETOM     3          ;Preload ac3 with -1,-1
2315 031443 201 01 0 00 000100      MOVEI     1,ZZ      ;Preload ac1 with floating 1
2316 031444 201 02 0 00 000001      MOVEI     2,1        ;Setup index register
2317 031445 200 03 0 02 000000      MOVE      3,(2)      ;*Fwt from indexed location
2318 031446 302 03 0 00 000100      CAIE      3,ZZ      ;Test indexing
2319                                     STOP^
2320 031447 254 04 0 00 031450      HALT      .+1        ;Test failed if program halts here
2321 031450 324 00 0 00 031451      JUMPA     .+1        ;To loop change this instruction^
2322
2323 ;*****
2324
2325 ;This test verifies that index register addressing functions correctly.
2326 ;In this test, a move instruction using indexing is executed. the move
2327 ;Instruction should place the contents of the location specified by index
2328 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2329 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2330 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2331
2332                                     001210
2333                                     000200      SN=SN+1
2334                                     ZZ=ZZ+ZZ
2335                                     IFE      ZZ,<ZZ=1>
2336 031451 476 00 0 00 000003      SETOM     3          ;Preload ac3 with -1,-1
2337 031452 201 01 0 00 000200      MOVEI     1,ZZ      ;Preload ac1 with floating 1
2338 031453 201 02 0 00 000001      MOVEI     2,1        ;Setup index register
2339 031454 200 03 0 02 000000      MOVE      3,(2)      ;*Fwt from indexed location
2340 031455 302 03 0 00 000200      CAIE      3,ZZ      ;Test indexing
2341                                     STOP^
2342 031456 254 04 0 00 031457      HALT      .+1        ;Test failed if program halts here
2343 031457 324 00 0 00 031460      JUMPA     .+1        ;To loop change this instruction^
2344
2345 ;*****

```

```

2346
2347
2348 ;This test verifies that index register addressing functions correctly.
2349 ;In this test, a move instruction using indexing is executed. the move
2350 ;Instruction should place the contents of the location specified by index
2351 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2352 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2353 ;Floating 1. if c(ac3)=a floating 1, this test passes
2354
2355 001211
2356 000400
2357
2358 031460 476 00 0 00 000003
2359 031461 201 01 0 00 000400
2360 031462 201 02 0 00 000001
2361 031463 200 03 0 02 000000
2362 031464 302 03 0 00 000400
2363
2364 031465 254 04 0 00 031466
2365 031466 324 00 0 00 031467
2366
2367
2368
2369
2370 ;*****
2371 ;This test verifies that index register addressing functions correctly.
2372 ;In this test, a move instruction using indexing is executed. the move
2373 ;Instruction should place the contents of the location specified by index
2374 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2375 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2376 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2377
2378 001212
2379 001000
2380
2381 031467 476 00 0 00 000003
2382 031470 201 01 0 00 001000
2383 031471 201 02 0 00 000001
2384 031472 200 03 0 02 000000
2385 031473 302 03 0 00 001000
2386
2387 031474 254 04 0 00 031475
2388 031475 324 00 0 00 031476
2389
2390
2391
2392 ;*****
2393 ;This test verifies that index register addressing functions correctly.
2394 ;In this test, a move instruction using indexing is executed. the move
2395 ;Instruction should place the contents of the location specified by index
2396 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2397 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2398 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2399
2400 001213
2400 002000

```

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes

SN=SN+1

ZZ=ZZ+ZZ

IFE ZZ,<ZZ=1>

SETOM 3

MOVEI 1,ZZ

MOVEI 2,1

MOVE 3,(2)

CAIE 3,ZZ

STOP^

HALT .+1

JUMPA .+1

;Preload ac3 with -1,-1

;Preload ac1 with floating 1

;Setup index register

;*Fwt from indexed location

;Test indexing

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ

IFE ZZ,<ZZ=1>

SETOM 3

MOVEI 1,ZZ

MOVEI 2,1

MOVE 3,(2)

CAIE 3,ZZ

STOP^

HALT .+1

JUMPA .+1

;Preload ac3 with -1,-1

;Preload ac1 with floating 1

;Setup index register

;*Fwt from indexed location

;Test indexing

;Test failed if program halts here

;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ

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2401							IFE	ZZ,<ZZ=1>	
2402	031476	476	00	0	00	000003	SETOM	3	;Preload ac3 with -1,-1
2403	031477	201	01	0	00	002000	MOVEI	1,ZZ	;Preload ac1 with floating 1
2404	031500	201	02	0	00	000001	MOVEI	2,1	;Setup index register
2405	031501	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
2406	031502	302	03	0	00	002000	CAIE	3,ZZ	;Test indexing
2407							STOP^		
2408	031503	254	04	0	00	031504	HALT	.+1	;Test failed if program halts here
2409	031504	324	00	0	00	031505	JUMPA	.+1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
;In this test, a move instruction using indexing is executed. the move
;Instruction should place the contents of the location specified by index
;Register 2 into ac3. since index register 2 was preloaded with a 1 and
;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
;Floating 1. if c(ac3)=a floating 1, this test passes.

2420									
2421						001214	SN=SN+1		
2422						004000	ZZ=ZZ+ZZ		
2423							IFE	ZZ,<ZZ=1>	
2424	031505	476	00	0	00	000003	SETOM	3	;Preload ac3 with -1,-1
2425	031506	201	01	0	00	004000	MOVEI	1,ZZ	;Preload ac1 with floating 1
2426	031507	201	02	0	00	000001	MOVEI	2,1	;Setup index register
2427	031510	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
2428	031511	302	03	0	00	004000	CAIE	3,ZZ	;Test indexing
2429							STOP^		
2430	031512	254	04	0	00	031513	HALT	.+1	;Test failed if program halts here
2431	031513	324	00	0	00	031514	JUMPA	.+1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
;In this test, a move instruction using indexing is executed. the move
;Instruction should place the contents of the location specified by index
;Register 2 into ac3. since index register 2 was preloaded with a 1 and
;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
;Floating 1. if c(ac3)=a floating 1, this test passes.

2442									
2443						001215	SN=SN+1		
2444						010000	ZZ=ZZ+ZZ		
2445							IFE	ZZ,<ZZ=1>	
2446	031514	476	00	0	00	000003	SETOM	3	;Preload ac3 with -1,-1
2447	031515	201	01	0	00	010000	MOVEI	1,ZZ	;Preload ac1 with floating 1
2448	031516	201	02	0	00	000001	MOVEI	2,1	;Setup index register
2449	031517	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
2450	031520	302	03	0	00	010000	CAIE	3,ZZ	;Test indexing
2451							STOP^		
2452	031521	254	04	0	00	031522	HALT	.+1	;Test failed if program halts here
2453	031522	324	00	0	00	031523	JUMPA	.+1	;To loop change this instruction^

;*****


```

2456
2457
2458 ;This test verifies that index register addressing functions correctly.
2459 ;In this test, a move instruction using indexing is executed. the move
2460 ;Instruction should place the contents of the location specified by index
2461 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2462 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2463 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2464
2465             001216
2466             020000
2467
2468 031523 476 00 0 00 000003
2469 031524 201 01 0 00 020000
2470 031525 201 02 0 00 000001
2471 031526 200 03 0 02 000000
2472 031527 302 03 0 00 020000
2473
2474 031530 254 04 0 00 031531
2475 031531 324 00 0 00 031532
2476
2477
2478
2479
2480
2481 ;This test verifies that index register addressing functions correctly.
2482 ;In this test, a move instruction using indexing is executed. the move
2483 ;Instruction should place the contents of the location specified by index
2484 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2485 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2486 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2487
2488             001217
2489             040000
2490
2491 031532 476 00 0 00 000003
2492 031533 201 01 0 00 040000
2493 031534 201 02 0 00 000001
2494 031535 200 03 0 02 000000
2495 031536 302 03 0 00 040000
2496
2497 031537 254 04 0 00 031540
2498 031540 324 00 0 00 031541
2499
2500
2501
2502
2503 ;This test verifies that index register addressing functions correctly.
2504 ;In this test, a move instruction using indexing is executed. the move
2505 ;Instruction should place the contents of the location specified by index
2506 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2507 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2508 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2509
2510             001220
                100000
    
```

SN=SN+1

```

ZZ=ZZ+ZZ
IFE      ZZ,<ZZ=1>
SETOM    3
MOVEI    1,ZZ
MOVEI    2,1
MOVE     3,(2)
CAIE     3,ZZ
STOP^
HALT     .+1
JUMPA    .+1
    
```

;*****

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

SN=SN+1

```

ZZ=ZZ+ZZ
IFE      ZZ,<ZZ=1>
SETOM    3
MOVEI    1,ZZ
MOVEI    2,1
MOVE     3,(2)
CAIE     3,ZZ
STOP^
HALT     .+1
JUMPA    .+1
    
```

;*****

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

SN=SN+1

```

ZZ=ZZ+ZZ
    
```



```

2511                                     IFE      ZZ,<ZZ=1>
2512 031541 476 00 0 00 000003        SETOM    3                ;Preload ac3 with -1,-1
2513 031542 201 01 0 00 100000        MOVEI    1,ZZ            ;Preload ac1 with floating 1
2514 031543 201 02 0 00 000001        MOVEI    2,1            ;Setup index register
2515 031544 200 03 0 02 000000        MOVE      3,(2)          ;*Fwt from indexed location
2516 031545 302 03 0 00 100000        CAIE     3,ZZ            ;Test indexing
2517                                     STOP^
2518 031546 254 04 0 00 031547        HALT      .+1              ;Test failed if program halts here
2519 031547 324 00 0 00 031550        JUMPA     .+1              ;To loop change this instruction^
2520
2521 ;*****
2522
2523
2524 ;This test verifies that index register addressing functions correctly.
2525 ;In this test, a move instruction using indexing is executed. the move
2526 ;Instruction should place the contents of the location specified by index
2527 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2528 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2529 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2530
2531                                     001221
2532                                     200000
2533                                     SN=SN+1
2534                                     ZZ=ZZ+ZZ
2535                                     IFE      ZZ,<ZZ=1>
2536 031550 476 00 0 00 000003        SETOM    3                ;Preload ac3 with -1,-1
2537 031551 201 01 0 00 200000        MOVEI    1,ZZ            ;Preload ac1 with floating 1
2538 031552 201 02 0 00 000001        MOVEI    2,1            ;Setup index register
2539 031553 200 03 0 02 000000        MOVE      3,(2)          ;*Fwt from indexed location
2540 031554 302 03 0 00 200000        CAIE     3,ZZ            ;Test indexing
2541                                     STOP^
2542 031555 254 04 0 00 031556        HALT      .+1              ;Test failed if program halts here
2543 031556 324 00 0 00 031557        JUMPA     .+1              ;To loop change this instruction^
2544
2545 ;*****
2546
2547 ;This test verifies that index register addressing functions correctly.
2548 ;In this test, a move instruction using indexing is executed. the move
2549 ;Instruction should place the contents of the location specified by index
2550 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2551 ;Ac1 was preloaded with a floating 1. the final result in ac3 should be a
2552 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2553
2554                                     001222
2555                                     400000
2556                                     SN=SN+1
2557                                     ZZ=ZZ+ZZ
2558                                     IFE      ZZ,<ZZ=1>
2559 031557 476 00 0 00 000003        SETOM    3                ;Preload ac3 with -1,-1
2560 031560 201 01 0 00 400000        MOVEI    1,ZZ            ;Preload ac1 with floating 1
2561 031561 201 02 0 00 000001        MOVEI    2,1            ;Setup index register
2562 031562 200 03 0 02 000000        MOVE      3,(2)          ;*Fwt from indexed location
2563 031563 302 03 0 00 400000        CAIE     3,ZZ            ;Test indexing
2564                                     STOP^
2565 031564 254 04 0 00 031565        HALT      .+1              ;Test failed if program halts here
2566 031565 324 00 0 00 031566        JUMPA     .+1              ;To loop change this instruction^
2567
2568 ;*****
    
```

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SEQ 0062

2566

```

2567          001300      SN=1300
2568          000000      ZZ=0
2569
2570      C1300: REPEAT ^D18,<
2571      ;This test verifies that index register addressing functions correctly.
2572      ;In this test, a move instruction using indexing is executed. the move
2573      ;Instruction should place the contents of the location specified by index
2574      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2575      ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2576      ;Floating 1. if c(ac3)=a floating 1, this test passes.
2577
2578      SN=SN+1
2579      ZZ=ZZ+ZZ
2580      IFE      ZZ,<ZZ=1>
2581      SETOM    3
2582      MOVSI    1,ZZ
2583      MOVEI    2,1
2584      MOVE     3,(2)
2585      CAME     3,[ZZ,,0]
2586      STOP
2587
2588      ;*****
2589      >
2590
2591      ;This test verifies that index register addressing functions correctly.
2592      ;In this test, a move instruction using indexing is executed. the move
2593      ;Instruction should place the contents of the location specified by index
2594      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2595      ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2596      ;Floating 1. if c(ac3)=a floating 1, this test passes.
2597
2598          001301      SN=SN+1
2599          000000      ZZ=ZZ+ZZ
2600          000001      IFE      ZZ,<ZZ=1>
2601      031566  476 00 0 00 000003      SETOM    3
2602      031567  205 01 0 00 000001      MOVSI    1,ZZ
2603      031570  201 02 0 00 000001      MOVEI    2,1
2604      031571  200 03 0 02 000000      MOVE     3,(2)
2605      031572  312 03 0 00 034421      CAME     3,[ZZ,,0]
2606
2607      031573  254 04 0 00 031574      STOP^
2608      031574  324 00 0 00 031575      HALT     .+1
2609
2610      ;*****
2611
2612      ;This test verifies that index register addressing functions correctly.
2613      ;In this test, a move instruction using indexing is executed. the move
2614      ;Instruction should place the contents of the location specified by index
2615      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2616      ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2617      ;Floating 1. if c(ac3)=a floating 1, this test passes.
2618
2619          001302      SN=SN+1
2620          000002      ZZ=ZZ+ZZ
2621

```

```
2622                                     IFE      ZZ,<ZZ=1>
2623 031575 476 00 0 00 000003          SETOM    3                ;Preload ac3 with -1,-1
2624 031576 205 01 0 00 000002          MOVSI    1,ZZ          ;Preload ac1 with floating 1
2625 031577 201 02 0 00 000001          MOVEI    2,1            ;Setup index register
2626 031600 200 03 0 02 000000          MOVE     3,(2)          ;*Fwt from indexed location
2627 031601 312 03 0 00 034422          CAME     3,[ZZ,,0]        ;Test indexing
2628                                     STOP^
2629 031602 254 04 0 00 031603          HALT     .+1          ;Test failed if program halts here
2630 031603 324 00 0 00 031604          JUMPA    .+1          ;To loop change this instruction^
2631
2632 ;*****
2633
2634 ;This test verifies that index register addressing functions correctly.
2635 ;In this test, a move instruction using indexing is executed. the move
2636 ;Instruction should place the contents of the location specified by index
2637 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2638 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2639 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2640
2641                                     001303
2642                                     000004
2643 SN=SN+1
2644                                     ZZ=ZZ+ZZ
2645 031604 476 00 0 00 000003          IFE      ZZ,<ZZ=1>
2646 031605 205 01 0 00 000004          SETOM    3                ;Preload ac3 with -1,-1
2647 031606 201 02 0 00 000001          MOVSI    1,ZZ          ;Preload ac1 with floating 1
2648 031607 200 03 0 02 000000          MOVEI    2,1            ;Setup index register
2649 031610 312 03 0 00 034423          MOVE     3,(2)          ;*Fwt from indexed location
2650                                     CAME     3,[ZZ,,0]        ;Test indexing
2651 031611 254 04 0 00 031612          STOP^
2652 031612 324 00 0 00 031613          HALT     .+1          ;Test failed if program halts here
2653                                     JUMPA    .+1          ;To loop change this instruction^
2654
2655 ;*****
2656
2657 ;This test verifies that index register addressing functions correctly.
2658 ;In this test, a move instruction using indexing is executed. the move
2659 ;Instruction should place the contents of the location specified by index
2660 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2661 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2662 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2663
2664                                     001304
2665                                     000010
2666 SN=SN+1
2667                                     ZZ=ZZ+ZZ
2668 031613 476 00 0 00 000003          IFE      ZZ,<ZZ=1>
2669 031614 205 01 0 00 000010          SETOM    3                ;Preload ac3 with -1,-1
2670 031615 201 02 0 00 000001          MOVSI    1,ZZ          ;Preload ac1 with floating 1
2671 031616 200 03 0 02 000000          MOVEI    2,1            ;Setup index register
2672 031617 312 03 0 00 034424          MOVE     3,(2)          ;*Fwt from indexed location
2673                                     CAME     3,[ZZ,,0]        ;Test indexing
2674 031620 254 04 0 00 031621          STOP^
2675 031621 324 00 0 00 031622          HALT     .+1          ;Test failed if program halts here
2676                                     JUMPA    .+1          ;To loop change this instruction^
2677
2678 ;*****
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001305
000020

031622	476	00	0	00	000003
031623	205	01	0	00	000020
031624	201	02	0	00	000001
031625	200	03	0	02	000000
031626	312	03	0	00	034425
031627	254	04	0	00	031630
031630	324	00	0	00	031631

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

SN=SN+1

ZZ=ZZ+ZZ
 IFE ZZ,<ZZ=1>
 SETOM 3
 MOVSI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,0]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

001306
000040

031631	476	00	0	00	000003
031632	205	01	0	00	000040
031633	201	02	0	00	000001
031634	200	03	0	02	000000
031635	312	03	0	00	034426
031636	254	04	0	00	031637
031637	324	00	0	00	031640

SN=SN+1

ZZ=ZZ+ZZ
 IFE ZZ,<ZZ=1>
 SETOM 3
 MOVSI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,0]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

001307
000100

SN=SN+1

ZZ=ZZ+ZZ

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2732                                     IFE      ZZ,<ZZ=1>
2733 031640 476 00 0 00 000003          SETOM    3                ;Preload ac3 with -1,-1
2734 031641 205 01 0 00 000100          MOVSI    1,ZZ            ;Preload ac1 with floating 1
2735 031642 201 02 0 00 000001          MOVEI    2,1              ;Setup index register
2736 031643 200 03 0 02 000000          MOVE     3,(2)            ;*Fwt from indexed location
2737 031644 312 03 0 00 034427          CAME     3,[ZZ,.0]        ;Test indexing
2738                                     STOP^
2739 031645 254 04 0 00 031646          HALT     .+1                ;Test failed if program halts here
2740 031646 324 00 0 00 031647          JUMPA    .+1                ;To loop change this instruction^
2741
2742 ;*****
2743
2744 ;This test verifies that index register addressing functions correctly.
2745 ;In this test, a move instruction using indexing is executed. the move
2746 ;Instruction should place the contents of the location specified by index
2747 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2748 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2749 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2750
2751                                     SN=SN+1
2752                                     ZZ=ZZ+ZZ
2753                                     IFE      ZZ,<ZZ=1>
2754                                     SETOM    3                ;Preload ac3 with -1,-1
2755 031647 476 00 0 00 000003          MOVSI    1,ZZ            ;Preload ac1 with floating 1
2756 031650 205 01 0 00 000200          MOVEI    2,1              ;Setup index register
2757 031651 201 02 0 00 000001          MOVE     3,(2)            ;*Fwt from indexed location
2758 031652 200 03 0 02 000000          CAME     3,[ZZ,.0]        ;Test indexing
2759 031653 312 03 0 00 034430          STOP^
2760                                     HALT     .+1                ;Test failed if program halts here
2761 031654 254 04 0 00 031655          JUMPA    .+1                ;To loop change this instruction^
2762 031655 324 00 0 00 031656
2763
2764 ;*****
2765
2766 ;This test verifies that index register addressing functions correctly.
2767 ;In this test, a move instruction using indexing is executed. the move
2768 ;Instruction should place the contents of the location specified by index
2769 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2770 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2771 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2772
2773                                     SN=SN+1
2774                                     ZZ=ZZ+ZZ
2775                                     IFE      ZZ,<ZZ=1>
2776                                     SETOM    3                ;Preload ac3 with -1,-1
2777 031656 476 00 0 00 000003          MOVSI    1,ZZ            ;Preload ac1 with floating 1
2778 031657 205 01 0 00 000400          MOVEI    2,1              ;Setup index register
2779 031660 201 02 0 00 000001          MOVE     3,(2)            ;*Fwt from indexed location
2780 031661 200 03 0 02 000000          CAME     3,[ZZ,.0]        ;Test indexing
2781 031662 312 03 0 00 034431          STOP^
2782                                     HALT     .+1                ;Test failed if program halts here
2783 031663 254 04 0 00 031664          JUMPA    .+1                ;To loop change this instruction^
2784 031664 324 00 0 00 031665
2785
2786 ;*****

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001312
 001000

031665	476	00	0	00	000003
031666	205	01	0	00	001000
031667	201	02	0	00	000001
031670	200	03	0	02	000000
031671	312	03	0	00	034432
031672	254	04	0	00	031673
031673	324	00	0	00	031674

SN=SN+1

ZZ=ZZ+ZZ
 IFE ZZ,<ZZ=1>
 SETOM 3
 MOVSI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,0]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with -1,,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

001313
 002000

031674	476	00	0	00	000003
031675	205	01	0	00	002000
031676	201	02	0	00	000001
031677	200	03	0	02	000000
031700	312	03	0	00	034433
031701	254	04	0	00	031702
031702	324	00	0	00	031703

SN=SN+1

ZZ=ZZ+ZZ
 IFE ZZ,<ZZ=1>
 SETOM 3
 MOVSI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,0]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with -1,,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

001314
 004000

SN=SN+1

ZZ=ZZ+ZZ

2842						IFE	ZZ,<ZZ=1>	
2843	031703	476	00	0	00	SETOM	3	;Preload ac3 with -1,-1
2844	031704	205	01	0	00	MOVSI	1,ZZ	;Preload ac1 with floating 1
2845	031705	201	02	0	00	MOVEI	2,1	;Setup index register
2846	031706	200	03	0	02	MOVE	3,(2)	;*Fwt from indexed location
2847	031707	312	03	0	00	CAME	3,[ZZ,.0]	;Test indexing
2848						STOP^		
2849	031710	254	04	0	00	HALT	+.1	;Test failed if program halts here
2850	031711	324	00	0	00	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

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2865	031712	476	00	0	00	IFE	ZZ,<ZZ=1>	
2866	031713	205	01	0	00	SETOM	3	;Preload ac3 with -1,-1
2867	031714	201	02	0	00	MOVSI	1,ZZ	;Preload ac1 with floating 1
2868	031715	200	03	0	02	MOVEI	2,1	;Setup index register
2869	031716	312	03	0	00	MOVE	3,(2)	;*Fwt from indexed location
2870						CAME	3,[ZZ,.0]	;Test indexing
2871	031717	254	04	0	00	STOP^		
2872	031720	324	00	0	00	HALT	+.1	;Test failed if program halts here
2873						JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

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2887	031721	476	00	0	00	IFE	ZZ,<ZZ=1>	
2888	031722	205	01	0	00	SETOM	3	;Preload ac3 with -1,-1
2889	031723	201	02	0	00	MOVSI	1,ZZ	;Preload ac1 with floating 1
2890	031724	200	03	0	02	MOVEI	2,1	;Setup index register
2891	031725	312	03	0	00	MOVE	3,(2)	;*Fwt from indexed location
2892						CAME	3,[ZZ,.0]	;Test indexing
2893	031726	254	04	0	00	STOP^		
2894	031727	324	00	0	00	HALT	+.1	;Test failed if program halts here
2895						JUMPA	+.1	;To loop change this instruction^

;*****

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001317
040000
031730 476 00 0 00 000003
031731 205 01 0 00 040000
031732 201 02 0 00 000001
031733 200 03 0 02 000000
031734 312 03 0 00 034437
031735 254 04 0 00 031736
031736 324 00 0 00 031737

001320
100000
031737 476 00 0 00 000003
031740 205 01 0 00 100000
031741 201 02 0 00 000001
031742 200 03 0 02 000000
031743 312 03 0 00 034440
031744 254 04 0 00 031745
031745 324 00 0 00 031746

001321
200000
    
```

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

```

SN=SN+1
ZZ=ZZ+ZZ
IFE ZZ,<ZZ=1>
SETOM 3
MOVSI 1,ZZ
MOVEI 2,1
MOVE 3,(2)
CAME 3,[ZZ,,0]
STOP^
HALT .+1
JUMPA .+1
    
```

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

```

SN=SN+1
ZZ=ZZ+ZZ
IFE ZZ,<ZZ=1>
SETOM 3
MOVSI 1,ZZ
MOVEI 2,1
MOVE 3,(2)
CAME 3,[ZZ,,0]
STOP^
HALT .+1
JUMPA .+1
    
```

;Preload ac3 with -1,-1
 ;Preload ac1 with floating 1
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
 ;Floating 1. if c(ac3)=a floating 1, this test passes.

```

SN=SN+1
ZZ=ZZ+ZZ
    
```

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2952                                     IFE      ZZ,<ZZ=1>
2953 031746 476 00 0 00 000003          SETOM    3                      ;Preload ac3 with -1,-1
2954 031747 205 01 0 00 200000          MOVSI    1,ZZ                      ;Preload ac1 with floating 1
2955 031750 201 02 0 00 000001          MOVEI    2,1                      ;Setup index register
2956 031751 200 03 0 02 000000          MOVE     3,(2)                    ;*Fwt from indexed location
2957 031752 312 03 0 00 034441          CAME     3,[ZZ,,0]                ;Test indexing
2958                                     STOP^
2959 031753 254 04 0 00 031754          HALT     .+1                      ;Test failed if program halts here
2960 031754 324 00 0 00 031755          JUMPA    .+1                      ;To loop change this instruction^
2961
2962 ;*****
2963
2964
2965 ;This test verifies that index register addressing functions correctly.
2966 ;In this test, a move instruction using indexing is executed. the move
2967 ;Instruction should place the contents of the location specified by index
2968 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2969 ;Ac1 was preloaded with a floating 1, the final result in ac3 should be a
2970 ;Floating 1. if c(ac3)=a floating 1, this test passes.
2971
2972                                     001322
2973                                     400000
2974                                     SN=SN+1
2975                                     ZZ=ZZ+ZZ
2976 031755 476 00 0 00 000003          IFE      ZZ,<ZZ=1>
2977 031756 205 01 0 00 400000          SETOM    3                      ;Preload ac3 with -1,-1
2978 031757 201 02 0 00 000001          MOVSI    1,ZZ                      ;Preload ac1 with floating 1
2979 031760 200 03 0 02 000000          MOVEI    2,1                      ;Setup index register
2980 031761 312 03 0 00 034442          MOVE     3,(2)                    ;*Fwt from indexed location
2981 031762 254 04 0 00 031763          CAME     3,[ZZ,,0]                ;Test indexing
2982 031763 324 00 0 00 031764          STOP^
2983                                     HALT     .+1                      ;Test failed if program halts here
2984                                     JUMPA    .+1                      ;To loop change this instruction^
2985 ;*****

```

```

2986 ;This test verifies that index register addressing functions correctly.
2987 ;In this test, a move instruction using indexing is executed. the move
2988 ;Instruction should place the contents of the location specified by index
2989 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
2990 ;Ac1 was preloaded with -1,, -1, the final result in ac3 should be -1,, -1.
2991 ;If c(ac3)=-1,, -1, this test passes.
2992
2993 031764 402 00 0 00 000003 C1400: SETZM 3 ;Preload ac3 with 0
2994 031765 476 00 0 00 000001 SETOM 1 ;Preload ac1 with -1,, -1
2995 031766 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
2996 031767 200 03 0 02 000000 MOVE 3,(2) ;*Fwt from indexed location
2997 031770 312 03 0 00 034443 CAME 3,[-1,, -1] ;Test indexing
2998 STOP^
2999 031771 254 04 0 00 031772 HALT .+1 ;Test failed if program halts here
3000 031772 324 00 0 00 031773 JUMPA .+1 ;To loop change this instruction^
3001
3002 ;*****
3003
3004 001500 SN=1500
3005 000000 ZZ=0
3006
3007 C1500: REPEAT ^D18,<
3008 ;This test verifies that index register addressing functions correctly.
3009 ;In this test, a move instruction using indexing is executed. the move
3010 ;Instruction should place the contents of the location specified by index
3011 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3012 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3013 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3014
3015 SN=SN+1
3016 ZZ=<ZZ+ZZ+1>&777777
3017 IFE <ZZ-1>,<ZZ=777776>
3018 SETZM 3 ;Preload ac3 with 0
3019 HRROI 1,ZZ ;Preload ac1 with floating 0
3020 MOVEI 2,1 ;Setup index register
3021 MOVE 3,(2) ;*Fwt from indexed location
3022 CAME 3,[-1,,ZZ] ;Test indexing
3023 STOP
3024
3025 ;*****
3026 >
3027
3028 ;This test verifies that index register addressing functions correctly.
3029 ;In this test, a move instruction using indexing is executed. the move
3030 ;Instruction should place the contents of the location specified by index
3031 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3032 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3033 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3034
3035 001501 SN=SN+1
3036 000001 ZZ=<ZZ+ZZ+1>&777777
3037 777776 IFE <ZZ-1>,<ZZ=777776>
3038 031773 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3039 031774 561 01 0 00 777776 HRROI 1,ZZ ;Preload ac1 with floating 0
3040 031775 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
  
```


3041	031776	200 03 0 02 000000	MOVE	3,(2)	;*Fwt from indexed location
3042	031777	312 03 0 00 034444	CAME	3,[-1,,ZZ]	;Test indexing
3043			STOP^		
3044	032000	254 04 0 00 032001	HALT	+.1	;Test failed if program halts here
3045	032001	324 00 0 00 032002	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001502
 777775

SN=SN+1

ZZ=<ZZ+ZZ+1>8777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRROI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[-1,,ZZ]
 STOP^
 HALT +.1
 JUMPA +.1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001503
 777773

SN=SN+1

ZZ=<ZZ+ZZ+1>8777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRROI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[-1,,ZZ]
 STOP^
 HALT +.1
 JUMPA +.1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move

3041 031776 200 03 0 02 000000
 3042 031777 312 03 0 00 034444
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 3044 032000 254 04 0 00 032001
 3045 032001 324 00 0 00 032002
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 3060 032002 402 00 0 00 000003
 3061 032003 561 01 0 00 777775
 3062 032004 201 02 0 00 000001
 3063 032005 200 03 0 02 000000
 3064 032006 312 03 0 00 034445
 3065
 3066 032007 254 04 0 00 032010
 3067 032010 324 00 0 00 032011
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 3082 032011 402 00 0 00 000003
 3083 032012 561 01 0 00 777773
 3084 032013 201 02 0 00 000001
 3085 032014 200 03 0 02 000000
 3086 032015 312 03 0 00 034446
 3087
 3088 032016 254 04 0 00 032017
 3089 032017 324 00 0 00 032020
 3090
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3096							;Instruction should place the contents of the location specified by index
3097							;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3098							;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3099							;Floating 0. if c(ac3)=a floating 0, this test passes.
3100							
3101				001504			SN=SN+1
3102				777767			ZZ=<ZZ+ZZ+1>&777777
3103							IFE <ZZ-1>,<ZZ=777776>
3104	032020	402	00	0	00	000003	SETZM 3 ;Preload ac3 with 0
3105	032021	561	01	0	00	777767	HRROI 1,ZZ ;Preload ac1 with floating 0
3106	032022	201	02	0	00	000001	MOVEI 2,1 ;Setup index register
3107	032023	200	03	0	02	000000	MOVE 3,(2) ;*Fwt from indexed location
3108	032024	312	03	0	00	034447	CAME 3,[-1,,ZZ] ;Test indexing
3109							STOP^
3110	032025	254	04	0	00	032026	HALT .+1 ;Test failed if program halts here
3111	032026	324	00	0	00	032027	JUMPA .+1 ;To loop change this instruction^
3112							
3113							:*****
3114							
3115							
3116							;This test verifies that index register addressing functions correctly.
3117							;In this test, a move instruction using indexing is executed. the move
3118							;Instruction should place the contents of the location specified by index
3119							;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3120							;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3121							;Floating 0. if c(ac3)=a floating 0, this test passes.
3122							
3123				001505			SN=SN+1
3124				777757			ZZ=<ZZ+ZZ+1>&777777
3125							IFE <ZZ-1>,<ZZ=777776>
3126	032027	402	00	0	00	000003	SETZM 3 ;Preload ac3 with 0
3127	032030	561	01	0	00	777757	HRROI 1,ZZ ;Preload ac1 with floating 0
3128	032031	201	02	0	00	000001	MOVEI 2,1 ;Setup index register
3129	032032	200	03	0	02	000000	MOVE 3,(2) ;*Fwt from indexed location
3130	032033	312	03	0	00	034450	CAME 3,[-1,,ZZ] ;Test indexing
3131							STOP^
3132	032034	254	04	0	00	032035	HALT .+1 ;Test failed if program halts here
3133	032035	324	00	0	00	032036	JUMPA .+1 ;To loop change this instruction^
3134							
3135							:*****
3136							
3137							
3138							;This test verifies that index register addressing functions correctly.
3139							;In this test, a move instruction using indexing is executed. the move
3140							;Instruction should place the contents of the location specified by index
3141							;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3142							;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3143							;Floating 0. if c(ac3)=a floating 0, this test passes.
3144							
3145				001506			SN=SN+1
3146				777737			ZZ=<ZZ+ZZ+1>&777777
3147							IFE <ZZ-1>,<ZZ=777776>
3148	032036	402	00	0	00	000003	SETZM 3 ;Preload ac3 with 0
3149	032037	561	01	0	00	777737	HRROI 1,ZZ ;Preload ac1 with floating 0
3150	032040	201	02	0	00	000001	MOVEI 2,1 ;Setup index register

3151	032041	200 03 0 02 000000	MOVE	3,(2)	;*Fwt from indexed location
3152	032042	312 03 0 00 034451	CAME	3,[-1,,ZZ]	;Test indexing
3153			STOP^		
3154	032043	254 04 0 00 032044	HALT	+.1	;Test failed if program halts here
3155	032044	324 00 0 00 032045	JUMPA	+.1	;To loop change this instruction^

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3166					
3167		001507			
3168		777677			
3169			SN=SN+1	ZZ=<ZZ+ZZ+1>8777777	
3170	032045	402 00 0 00 000003	IFE	<ZZ-1>,<ZZ=777776>	
3171	032046	561 01 0 00 777677	SETZM	3	;Preload ac3 with 0
3172	032047	201 02 0 00 000001	HRROI	1,ZZ	;Preload ac1 with floating 0
3173	032050	200 03 0 02 000000	MOVEI	2,1	;Setup index register
3174	032051	312 03 0 00 034452	MOVE	3,(2)	;*Fwt from indexed location
3175			CAME	3,[-1,,ZZ]	;Test indexing
3176	032052	254 04 0 00 032053	STOP^		
3177	032053	324 00 0 00 032054	HALT	+.1	;Test failed if program halts here
3178			JUMPA	+.1	;To loop change this instruction^

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3188					
3189		001510			
3190		777577			
3191			SN=SN+1	ZZ=<ZZ+ZZ+1>8777777	
3192	032054	402 00 0 00 000003	IFE	<ZZ-1>,<ZZ=777776>	
3193	032055	561 01 0 00 777577	SETZM	3	;Preload ac3 with 0
3194	032056	201 02 0 00 000001	HRROI	1,ZZ	;Preload ac1 with floating 0
3195	032057	200 03 0 02 000000	MOVEI	2,1	;Setup index register
3196	032060	312 03 0 00 034453	MOVE	3,(2)	;*Fwt from indexed location
3197			CAME	3,[-1,,ZZ]	;Test indexing
3198	032061	254 04 0 00 032062	STOP^		
3199	032062	324 00 0 00 032063	HALT	+.1	;Test failed if program halts here
3200			JUMPA	+.1	;To loop change this instruction^

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move

3205

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3206 ;Instruction should place the contents of the location specified by index
3207 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3208 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3209 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3210
3211 001511 SN=SN+1
3212 777377 ZZ=<ZZ+ZZ+1>&777777
3213 IFB <ZZ-1>,<ZZ=777776>
3214 032063 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3215 032064 561 01 0 00 777377 HRROI 1,ZZ ;Preload ac1 with floating 0
3216 032065 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
3217 032066 200 03 0 02 000000 MOVE 3,(2) ;*Fwt from indexed location
3218 032067 312 03 0 00 034454 CAME 3,[-1,,ZZ] ;Test indexing
3219 STOP^
3220 032070 254 04 0 00 032071 HALT .+1 ;Test failed if program halts here
3221 032071 324 00 0 00 032072 JUMPA .+1 ;To loop change this instruction^
3222
3223 ;*****
3224
3225 ;This test verifies that index register addressing functions correctly.
3226 ;In this test, a move instruction using indexing is executed. the move
3227 ;Instruction should place the contents of the location specified by index
3228 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3229 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3230 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3231
3232 001512 SN=SN+1
3233 776777 ZZ=<ZZ+ZZ+1>&777777
3234 IFB <ZZ-1>,<ZZ=777776>
3235 032072 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3236 032073 561 01 0 00 776777 HRROI 1,ZZ ;Preload ac1 with floating 0
3237 032074 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
3238 032075 200 03 0 02 000000 MOVE 3,(2) ;*Fwt from indexed location
3239 032076 312 03 0 00 034455 CAME 3,[-1,,ZZ] ;Test indexing
3240 STOP^
3241 032077 254 04 0 00 032100 HALT .+1 ;Test failed if program halts here
3242 032100 324 00 0 00 032101 JUMPA .+1 ;To loop change this instruction^
3243
3244 ;*****
3245
3246 ;This test verifies that index register addressing functions correctly.
3247 ;In this test, a move instruction using indexing is executed. the move
3248 ;Instruction should place the contents of the location specified by index
3249 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3250 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3251 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3252
3253 001513 SN=SN+1
3254 775777 ZZ=<ZZ+ZZ+1>&777777
3255 IFB <ZZ-1>,<ZZ=777776>
3256 032101 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3257 032102 561 01 0 00 775777 HRROI 1,ZZ ;Preload ac1 with floating 0
3258 032103 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
    
```


3261	032104	200 03 0 02 000000	MOVE	3,(2)	;*Fwt from indexed location
3262	032105	312 03 0 00 034456	CAME	3,[-1,,ZZ]	;Test indexing
3263			STOP^		
3264	032106	254 04 0 00 032107	HALT	+.1	;Test failed if program halts here
3265	032107	324 00 0 00 032110	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3277		001514	SN=SN+1		
3278		773777			
3279			ZZ=<ZZ+ZZ+1>&777777		
3280	032110	402 00 0 00 000003	IFE	<ZZ-1>,<ZZ=777776>	
3281	032111	561 01 0 00 773777	SETZM	3	;Preload ac3 with 0
3282	032112	201 02 0 00 000001	HRROI	1,ZZ	;Preload ac1 with floating 0
3283	032113	200 03 0 02 000000	MOVEI	2,1	;Setup index register
3284	032114	312 03 0 00 034457	MOVE	3,(2)	;*Fwt from indexed location
3285			CAME	3,[-1,,ZZ]	;Test indexing
3286	032115	254 04 0 00 032116	STOP^		
3287	032116	324 00 0 00 032117	HALT	+.1	;Test failed if program halts here
3288			JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3299		001515	SN=SN+1		
3300		767777			
3301			ZZ=<ZZ+ZZ+1>&777777		
3302	032117	402 00 0 00 000003	IFE	<ZZ-1>,<ZZ=777776>	
3303	032120	561 01 0 00 767777	SETZM	3	;Preload ac3 with 0
3304	032121	201 02 0 00 000001	HRROI	1,ZZ	;Preload ac1 with floating 0
3305	032122	200 03 0 02 000000	MOVEI	2,1	;Setup index register
3306	032123	312 03 0 00 034460	MOVE	3,(2)	;*Fwt from indexed location
3307			CAME	3,[-1,,ZZ]	;Test indexing
3308	032124	254 04 0 00 032125	STOP^		
3309	032125	324 00 0 00 032126	HALT	+.1	;Test failed if program halts here
3310			JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move

3315


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3316 ;Instruction should place the contents of the location specified by index
3317 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3318 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3319 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3320
3321 001516 SN=SN+1
3322 757777 ZZ=<ZZ+ZZ+1>&777777
3323 IFE <ZZ-1>,<ZZ=777776>
3324 032126 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3325 032127 561 01 0 00 757777 HRROI 1,ZZ ;Preload ac1 with floating 0
3326 032130 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
3327 032131 200 03 0 02 000000 MOVE 3,(2) ;*Fwt from indexed location
3328 032132 312 03 0 00 034461 CAME 3,[-1,,ZZ] ;Test indexing
3329 STOP^
3330 032133 254 04 0 00 032134 HALT .+1 ;Test failed if program halts here
3331 032134 324 00 0 00 032135 JUMPA .+1 ;To loop change this instruction^
3332
3333 ;*****
3334
3335 ;This test verifies that index register addressing functions correctly.
3336 ;In this test, a move instruction using indexing is executed. the move
3337 ;Instruction should place the contents of the location specified by index
3338 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3339 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3340 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3341
3342 001517 SN=SN+1
3343 737777 ZZ=<ZZ+ZZ+1>&777777
3344 IFE <ZZ-1>,<ZZ=777776>
3345 032135 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3346 032136 561 01 0 00 737777 HRROI 1,ZZ ;Preload ac1 with floating 0
3347 032137 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
3348 032140 200 03 0 02 000000 MOVE 3,(2) ;*Fwt from indexed location
3349 032141 312 03 0 00 034462 CAME 3,[-1,,ZZ] ;Test indexing
3350 STOP^
3351 032142 254 04 0 00 032143 HALT .+1 ;Test failed if program halts here
3352 032143 324 00 0 00 032144 JUMPA .+1 ;To loop change this instruction^
3353
3354 ;*****
3355
3356 ;This test verifies that index register addressing functions correctly.
3357 ;In this test, a move instruction using indexing is executed. the move
3358 ;Instruction should place the contents of the location specified by index
3359 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3360 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3361 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3362
3363 001520 SN=SN+1
3364 677777 ZZ=<ZZ+ZZ+1>&777777
3365 IFE <ZZ-1>,<ZZ=777776>
3366 032144 402 00 0 00 000003 SETZM 3 ;Preload ac3 with 0
3367 032145 561 01 0 00 677777 HRROI 1,ZZ ;Preload ac1 with floating 0
3368 032146 201 02 0 00 000001 MOVEI 2,1 ;Setup index register
  
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3371 032147 200 03 0 02 000000      MOVE    3,(2)          ;*Fwt from indexed location
3372 032150 312 03 0 00 034463      CAME    3,[-1,,ZZ]      ;Test indexing
3373                                     STOP^
3374 032151 254 04 0 00 032152      HALT     .+1          ;Test failed if program halts here
3375 032152 324 00 0 00 032153      JUMPA    .+1          ;To loop change this instruction^
3376
3377      ;*****
3378
3379      ;This test verifies that index register addressing functions correctly.
3380      ;In this test, a move instruction using indexing is executed. the move
3381      ;Instruction should place the contents of the location specified by index
3382      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3383      ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3384      ;Floating 0. if c(ac3)=a floating 0, this test passes.
3385
3386      001521
3387      577777
3388      SN=SN+1
3389      ZZ=<ZZ+ZZ+1>&777777
3390      IFE    <ZZ-1>,<ZZ=777776>
3391      SETZM   3
3392      HRROI   1,ZZ          ;Preload ac3 with 0
3393      MOVEI   2,1          ;Preload ac1 with floating 0
3394      MOVE    3,(2)          ;Setup index register
3395      CAME    3,[-1,,ZZ]      ;*Fwt from indexed location
3396      STOP^
3397      HALT     .+1          ;Test failed if program halts here
3398      JUMPA    .+1          ;To loop change this instruction^
3399
3400      ;*****
3401
3402      ;This test verifies that index register addressing functions correctly.
3403      ;In this test, a move instruction using indexing is executed. the move
3404      ;Instruction should place the contents of the location specified by index
3405      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3406      ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3407      ;Floating 0. if c(ac3)=a floating 0, this test passes.
3408
3409      001522
3410      377777
3411      SN=SN+1
3412      ZZ=<ZZ+ZZ+1>&777777
3413      IFE    <ZZ-1>,<ZZ=777776>
3414      SETZM   3
3415      HRROI   1,ZZ          ;Preload ac3 with 0
3416      MOVEI   2,1          ;Preload ac1 with floating 0
3417      MOVE    3,(2)          ;Setup index register
3418      CAME    3,[-1,,ZZ]      ;*Fwt from indexed location
3419      STOP^
3420      HALT     .+1          ;Test failed if program halts here
3421      JUMPA    .+1          ;To loop change this instruction^
3422
3423      ;*****
    
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3423          001600      SN=1600
3424          000000      ZZ=0
3425
3426      C1600: REPEAT ^D18,<
3427      ;This test verifies that index register addressing functions correctly.
3428      ;In this test, a move instruction using indexing is executed. the move
3429      ;Instruction should place the contents of the location specified by index
3430      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3431      ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3432      ;Floating 0. if c(ac3)=a floating 0, this test passes.
3433
3434      SN=SN+1
3435      ZZ=<ZZ+ZZ+1>&777777
3436      IFE      <ZZ-1>,<ZZ=777776>
3437      SETZM    3                      ;Preload ac3 with 0
3438      HRLOI    1,ZZ                  ;Preload ac1 with floating 0
3439      MOVEI    2,1                  ;Setup index register
3440      MOVE     3,(2)                ;*Fwt from indexed location
3441      CAME     3,[ZZ,,-1]           ;Test indexing
3442      STOP
3443
3444      ;*****
3445      >
3446
3447      ;This test verifies that index register addressing functions correctly.
3448      ;In this test, a move instruction using indexing is executed. the move
3449      ;Instruction should place the contents of the location specified by index
3450      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3451      ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3452      ;Floating 0. if c(ac3)=a floating 0, this test passes.
3453
3454          001601
3455          000001
3456          777776
3457      032171  402 00 0 00 000003
3458      032172  525 01 0 00 777776
3459      032173  201 02 0 00 000001
3460      032174  200 03 0 02 000000
3461      032175  312 03 0 00 034466
3462
3463      032176  254 04 0 00 032177
3464      032177  324 00 0 00 032200
3465
3466      SN=SN+1
3467      ZZ=<ZZ+ZZ+1>&777777
3468      IFE      <ZZ-1>,<ZZ=777776>
3469      SETZM    3                      ;Preload ac3 with 0
3470      HRLOI    1,ZZ                  ;Preload ac1 with floating 0
3471      MOVEI    2,1                  ;Setup index register
3472      MOVE     3,(2)                ;*Fwt from indexed location
3473      CAME     3,[ZZ,,-1]           ;Test indexing
3474      STOP^
3475      HALT     .+1                  ;Test failed if program halts here
3476      JUMPA    .+1                  ;To loop change this instruction^
3477
3478      ;*****
3479
3480      ;This test verifies that index register addressing functions correctly.
3481      ;In this test, a move instruction using indexing is executed. the move
3482      ;Instruction should place the contents of the location specified by index
3483      ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3484      ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3485      ;Floating 0. if c(ac3)=a floating 0, this test passes.
3486
3487          001602
3488          777775
3489      SN=SN+1
3490      ZZ=<ZZ+ZZ+1>&777777

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3478							IFE	<ZZ-1>,<ZZ=777776>	
3479	032200	402	00	0	00	000003	SETZM	3	;Preload ac3 with 0
3480	032201	525	01	0	00	777775	HRLOI	1,ZZ	;Preload ac1 with floating 0
3481	032202	201	02	0	00	000001	MOVEI	2,1	;Setup index register
3482	032203	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
3483	032204	312	03	0	00	034467	CAME	3,[ZZ,,-1]	;Test indexing
3484							STOP^		
3485	032205	254	04	0	00	032206	HALT	+.1	;Test failed if program halts here
3486	032206	324	00	0	00	032207	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001603
 777773

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777

3500							IFE	<ZZ-1>,<ZZ=777776>	
3501	032207	402	00	0	00	000003	SETZM	3	;Preload ac3 with 0
3502	032210	525	01	0	00	777773	HRLOI	1,ZZ	;Preload ac1 with floating 0
3503	032211	201	02	0	00	000001	MOVEI	2,1	;Setup index register
3504	032212	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
3505	032213	312	03	0	00	034470	CAME	3,[ZZ,,-1]	;Test indexing
3506							STOP^		
3507	032214	254	04	0	00	032215	HALT	+.1	;Test failed if program halts here
3508	032215	324	00	0	00	032216	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001604
 777767

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777

3520							IFE	<ZZ-1>,<ZZ=777776>	
3521							SETZM	3	;Preload ac3 with 0
3522							HRLOI	1,ZZ	;Preload ac1 with floating 0
3523	032216	402	00	0	00	000003	MOVEI	2,1	;Setup index register
3524	032217	525	01	0	00	777767	MOVE	3,(2)	;*Fwt from indexed location
3525	032220	201	02	0	00	000001	CAME	3,[ZZ,,-1]	;Test indexing
3526	032221	200	03	0	02	000000	STOP^		
3527	032222	312	03	0	00	034471	HALT	+.1	;Test failed if program halts here
3528							JUMPA	+.1	;To loop change this instruction^
3529	032223	254	04	0	00	032224			
3530	032224	324	00	0	00	032225			

;*****

3533
 3534
 3535
 3536
 3537
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001605
 777757

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,..-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001606
 777737

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,..-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001607
 777677

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777

3588							IFE	<ZZ-1>,<ZZ=777776>	
3589	032243	402	00	0	00	000003	SETZM	3	;Preload ac3 with 0
3590	032244	525	01	0	00	777677	HRLOI	1,ZZ	;Preload ac1 with floating 0
3591	032245	201	02	0	00	000001	MOVEI	2,1	;Setup index register
3592	032246	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
3593	032247	312	03	0	00	034474	CAME	3,[ZZ..-1]	;Test indexing
3594							STOP^		
3595	032250	254	04	0	00	032251	HALT	+.1	;Test failed if program halts here
3596	032251	324	00	0	00	032252	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3608						001610	SN=SN+1		
3609						777577		ZZ=<ZZ+ZZ+1>&777777	
3610							IFE	<ZZ-1>,<ZZ=777776>	
3611	032252	402	00	0	00	000003	SETZM	3	;Preload ac3 with 0
3612	032253	525	01	0	00	777577	HRLOI	1,ZZ	;Preload ac1 with floating 0
3613	032254	201	02	0	00	000001	MOVEI	2,1	;Setup index register
3614	032255	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
3615	032256	312	03	0	00	034475	CAME	3,[ZZ..-1]	;Test indexing
3616							STOP^		
3617	032257	254	04	0	00	032260	HALT	+.1	;Test failed if program halts here
3618	032260	324	00	0	00	032261	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

3630						001611	SN=SN+1		
3631						777377		ZZ=<ZZ+ZZ+1>&777777	
3632							IFE	<ZZ-1>,<ZZ=777776>	
3633	032261	402	00	0	00	000003	SETZM	3	;Preload ac3 with 0
3634	032262	525	01	0	00	777377	HRLOI	1,ZZ	;Preload ac1 with floating 0
3635	032263	201	02	0	00	000001	MOVEI	2,1	;Setup index register
3636	032264	200	03	0	02	000000	MOVE	3,(2)	;*Fwt from indexed location
3637	032265	312	03	0	00	034476	CAME	3,[ZZ..-1]	;Test indexing
3638							STOP^		
3639	032266	254	04	0	00	032267	HALT	+.1	;Test failed if program halts here
3640	032267	324	00	0	00	032270	JUMPA	+.1	;To loop change this instruction^

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001612
776777

032270	402	00	0	00	000003
032271	525	01	0	00	776777
032272	201	02	0	00	000001
032273	200	03	0	02	000000
032274	312	03	0	00	034477
032275	254	04	0	00	032276
032276	324	00	0	00	032277

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001613
775777

032277	402	00	0	00	000003
032300	525	01	0	00	775777
032301	201	02	0	00	000001
032302	200	03	0	02	000000
032303	312	03	0	00	034500
032304	254	04	0	00	032305
032305	324	00	0	00	032306

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001614
773777

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777


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3698                                     IFE      <ZZ-1>,<ZZ=777776>
3699 032306 402 00 0 00 000003          SETZM    3                      ;Preload ac3 with 0
3700 032307 525 01 0 00 773777          HRLOI    1,ZZ                  ;Preload ac1 with floating 0
3701 032310 201 02 0 00 000001          MOVEI    2,1                      ;Setup index register
3702 032311 200 03 0 02 000000          MOVE     3,(2)                  ;*Fwt from indexed location
3703 032312 312 03 0 00 034501          CAME     3,[ZZ,,-1]              ;Test indexing
3704                                     STOP^
3705 032313 254 04 0 00 032314          HALT     .+1                      ;Test failed if program halts here
3706 032314 324 00 0 00 032315          JUMPA    .+1                      ;To loop change this instruction^
3707
3708 ;*****
3709
3710
3711 ;This test verifies that index register addressing functions correctly.
3712 ;In this test, a move instruction using indexing is executed. the move
3713 ;Instruction should place the contents of the location specified by index
3714 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3715 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3716 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3717
3718                                     001615
3719                                     767777
3720 SN=SN+1
3721                                     ZZ=<ZZ+ZZ+1>&777777
3722 032315 402 00 0 00 000003          IFE      <ZZ-1>,<ZZ=777776>
3723 032316 525 01 0 00 767777          SETZM    3                      ;Preload ac3 with 0
3724 032317 201 02 0 00 000001          HRLOI    1,ZZ                  ;Preload ac1 with floating 0
3725 032320 200 03 0 02 000000          MOVEI    2,1                      ;Setup index register
3726 032321 312 03 0 00 034502          MOVE     3,(2)                  ;*Fwt from indexed location
3727                                     CAME     3,[ZZ,,-1]              ;Test indexing
3728 032322 254 04 0 00 032323          STOP^
3729 032323 324 00 0 00 032324          HALT     .+1                      ;Test failed if program halts here
3730                                     JUMPA    .+1                      ;To loop change this instruction^
3731
3732 ;*****
3733
3734 ;This test verifies that index register addressing functions correctly.
3735 ;In this test, a move instruction using indexing is executed. the move
3736 ;Instruction should place the contents of the location specified by index
3737 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3738 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3739 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3740
3741                                     001616
3742                                     757777
3743 SN=SN+1
3744                                     ZZ=<ZZ+ZZ+1>&777777
3745 032324 402 00 0 00 000003          IFE      <ZZ-1>,<ZZ=777776>
3746 032325 525 01 0 00 757777          SETZM    3                      ;Preload ac3 with 0
3747 032326 201 02 0 00 000001          HRLOI    1,ZZ                  ;Preload ac1 with floating 0
3748 032327 200 03 0 02 000000          MOVEI    2,1                      ;Setup index register
3749 032330 312 03 0 00 034503          MOVE     3,(2)                  ;*Fwt from indexed location
3750                                     CAME     3,[ZZ,,-1]              ;Test indexing
3751 032331 254 04 0 00 032332          STOP^
3752 032332 324 00 0 00 032333          HALT     .+1                      ;Test failed if program halts here
                                     JUMPA    .+1                      ;To loop change this instruction^
3753
3754 ;*****
    
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001617
 737777

032333	402	00	0	00	000003
032334	525	01	0	00	737777
032335	201	02	0	00	000001
032336	200	03	0	02	000000
032337	312	03	0	00	034504
032340	254	04	0	00	032341
032341	324	00	0	00	032342

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001620
 677777

032342	402	00	0	00	000003
032343	525	01	0	00	677777
032344	201	02	0	00	000001
032345	200	03	0	02	000000
032346	312	03	0	00	034505
032347	254	04	0	00	032350
032350	324	00	0	00	032351

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777
 IFE <ZZ-1>,<ZZ=777776>
 SETZM 3
 HRLOI 1,ZZ
 MOVEI 2,1
 MOVE 3,(2)
 CAME 3,[ZZ,,-1]
 STOP^
 HALT .+1
 JUMPA .+1

;Preload ac3 with 0
 ;Preload ac1 with floating 0
 ;Setup index register
 ;*Fwt from indexed location
 ;Test indexing
 ;Test failed if program halts here
 ;To loop change this instruction^

;*****

;This test verifies that index register addressing functions correctly.
 ;In this test, a move instruction using indexing is executed. the move
 ;Instruction should place the contents of the location specified by index
 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
 ;Floating 0. if c(ac3)=a floating 0, this test passes.

001621
 577777

SN=SN+1

ZZ=<ZZ+ZZ+1>&777777

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3808
3809 032351 402 00 0 00 000003      IFE      <ZZ-1>,<ZZ=777776>
3810 032352 525 01 0 00 577777      SETZM    3          ;Preload ac3 with 0
3811 032353 201 02 0 00 000001      HRLOI    1,ZZ      ;Preload ac1 with floating 0
3812 032354 200 03 0 02 000000      MOVEI    2,1      ;Setup index register
3813 032355 312 03 0 00 C34506      MOVE     3,(2)     ;*Fwt from indexed location
3814                                CAME     3,[ZZ,,-1]      ;Test indexing
3815                                STOP^
3816 032356 254 04 0 00 032357      HALT     .+1       ;Test failed if program halts here
3817 032357 324 00 0 00 032360      JUMPA    .+1       ;To loop change this instruction^
3818
3819 ;*****
3820
3821 ;This test verifies that index register addressing functions correctly.
3822 ;In this test, a move instruction using indexing is executed. the move
3823 ;Instruction should place the contents of the location specified by index
3824 ;Register 2 into ac3. since index register 2 was preloaded with a 1 and
3825 ;Ac1 was preloaded with a floating 0, the final result in ac3 should be a
3826 ;Floating 0. if c(ac3)=a floating 0, this test passes.
3827
3828                                001622
3829                                377777
3830                                SN=SN+1
3831                                ZZ=<ZZ+ZZ+1>8777777
3832 032360 402 00 0 00 000003      IFE      <ZZ-1>,<ZZ=777776>
3833 032361 525 01 0 00 377777      SETZM    3          ;Preload ac3 with 0
3834 032362 201 02 0 00 000001      HRLOI    1,ZZ      ;Preload ac1 with floating 0
3835 032363 200 03 0 02 000000      MOVEI    2,1      ;Setup index register
3836 032364 312 03 0 00 034507      MOVE     3,(2)     ;*Fwt from indexed location
3837                                CAME     3,[ZZ,,-1]      ;Test indexing
3838                                STOP^
3839 032365 254 04 0 00 032366      HALT     .+1       ;Test failed if program halts here
3840 032366 324 00 0 00 032367      JUMPA    .+1       ;To loop change this instruction^
3841
3842 ;*****
    
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3842 ;Verify indexing where 'e' is non-zero
3843
3844 SN=1700
3845 777777 001700 ZZ=-1
3846 777777 777777 XX=-10
3847
3848 ;This test verifies that index register addressing functions correctly. in
3849 ;This test, the index reg is set-up with movei zz+1,zz-xx, where zz+1 is the
3850 ;Index reg. the ac is preloaded with its own address, 0,,zz. caie is used to
3851 ;Test the indexing operation. if the result in c(ac)=xx+c(zz+1 - right), this
3852 ;Test passes. xx+c(zz+1 - right) should = zz.
3853
3854 C1700: REPEAT ^D15,
3855 <SN=SN+1
3856 ZZ=ZZ+1
3857 XX=XX+3
3858 MOVEI ZZ+1,ZZ-XX ;Setup index register
3859 MOVEI ZZ,ZZ ;Preload ac with 0,,zz
3860 CAIE ZZ,XX(ZZ+1) ;*Test indexing
3861 STOP
3862
3863 ;*****
3864 >
3865 SN=SN+1
3866 001701 ZZ=ZZ+1
3867 000000 XX=XX+3
3868 032367 201 01 0 00 000005 MOVEI ZZ+1,ZZ-XX ;Setup index register
3869 032370 201 00 0 00 000000 MOVEI ZZ,ZZ ;Preload ac with 0,,zz
3870 032371 302 00 0 01 777773 CAIE ZZ,XX(ZZ+1) ;*Test indexing
3871 STOP^
3872 032372 254 04 0 00 032373 HALT .+1 ;Test failed if program halts here
3873 032373 324 00 0 00 032374 JUMPA .+1 ;To loop change this instruction^
3874
3875 ;*****
3876
3877 SN=SN+1
3878 001702 ZZ=ZZ+1
3879 000001 XX=XX+3
3880 032374 201 02 0 00 000003 MOVEI ZZ+1,ZZ-XX ;Setup index register
3881 032375 201 01 0 00 000001 MOVEI ZZ,ZZ ;Preload ac with 0,,zz
3882 032376 302 01 0 02 777776 CAIE ZZ,XX(ZZ+1) ;*Test indexing
3883 STOP^
3884 032377 254 04 0 00 032400 HALT .+1 ;Test failed if program halts here
3885 032400 324 00 0 00 032401 JUMPA .+1 ;To loop change this instruction^
3886
3887 ;*****
3888
3889 SN=SN+1
3890 001703 ZZ=ZZ+1
3891 000002 XX=XX+3
3892 032401 201 03 0 00 000001 MOVEI ZZ+1,ZZ-XX ;Setup index register
3893 032402 201 02 0 00 000002 MOVEI ZZ,ZZ ;Preload ac with 0,,zz
3894 032403 302 02 0 03 000001 CAIE ZZ,XX(ZZ+1) ;*Test indexing
3895 STOP^
3896 032404 254 04 0 00 032405 HALT .+1 ;Test failed if program halts here
    
```

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3897 032405 324 00 0 00 032406          JUMPA      .+1          ;To loop change this instruction^
3898
3899          ;*****
3900
3901          001704          SN=SN+1
3902          000003          ZZ=ZZ+1
3903          000004          XX=XX+3
3904 032406 201 04 0 00 777777          MOVEI      ZZ+1,ZZ-XX          ;Setup index register
3905 032407 201 03 0 00 000003          MOVEI      ZZ,ZZ          ;Preload ac with 0,,zz
3906 032410 302 03 0 04 000004          CAIE       ZZ,XX(ZZ+1)          ;*Test indexing
3907          STOP^
3908 032411 254 04 0 00 032412          HALT       .+1          ;Test failed if program halts here
3909 032412 324 00 0 00 032413          JUMPA      .+1          ;To loop change this instruction^
3910
3911          ;*****
3912
3913          001705          SN=SN+1
3914          000004          ZZ=ZZ+1
3915          000007          XX=XX+3
3916 032413 201 05 0 00 777775          MOVEI      ZZ+1,ZZ-XX          ;Setup index register
3917 032414 201 04 0 00 000004          MOVEI      ZZ,ZZ          ;Preload ac with 0,,zz
3918 032415 302 04 0 05 000007          CAIE       ZZ,XX(ZZ+1)          ;*Test indexing
3919          STOP^
3920 032416 254 04 0 00 032417          HALT       .+1          ;Test failed if program halts here
3921 032417 324 00 0 00 032420          JUMPA      .+1          ;To loop change this instruction^
3922
3923          ;*****
3924
3925          001706          SN=SN+1
3926          000005          ZZ=ZZ+1
3927          000012          XX=XX+3
3928 032420 201 06 0 00 777773          MOVEI      ZZ+1,ZZ-XX          ;Setup index register
3929 032421 201 05 0 00 000005          MOVEI      ZZ,ZZ          ;Preload ac with 0,,zz
3930 032422 302 05 0 06 000012          CAIE       ZZ,XX(ZZ+1)          ;*Test indexing
3931          STOP^
3932 032423 254 04 0 00 032424          HALT       .+1          ;Test failed if program halts here
3933 032424 324 00 0 00 032425          JUMPA      .+1          ;To loop change this instruction^
3934
3935          ;*****
3936
3937          001707          SN=SN+1
3938          000006          ZZ=ZZ+1
3939          000015          XX=XX+3
3940 032425 201 07 0 00 777771          MOVEI      ZZ+1,ZZ-XX          ;Setup index register
3941 032426 201 06 0 00 000006          MOVEI      ZZ,ZZ          ;Preload ac with 0,,zz
3942 032427 302 06 0 07 000015          CAIE       ZZ,XX(ZZ+1)          ;*Test indexing
3943          STOP^
3944 032430 254 04 0 00 032431          HALT       .+1          ;Test failed if program halts here
3945 032431 324 00 0 00 032432          JUMPA      .+1          ;To loop change this instruction^
3946
3947          ;*****
3948
3949          001710          SN=SN+1
3950          000007          ZZ=ZZ+1
3951          000020          XX=XX+3
  
```


3952	032432	201	10	0	00	777767		MOVEI	ZZ+1,ZZ-XX	;Setup index register
3953	032433	201	07	0	00	000007		MOVEI	ZZ,ZZ	;Preload ac with 0,,zz
3954	032434	302	07	0	10	000020		CAIE	ZZ,XX(ZZ+1)	*Test indexing
3955								STOP^		
3956	032435	254	04	0	00	032436		HALT	.+1	;Test failed if program halts here
3957	032436	324	00	0	00	032437		JUMPA	.+1	;To loop change this instruction^
3958										
3959										
3960										
3961						001711	SN=SN+1			
3962						000010		ZZ=ZZ+1		
3963						000023		XX=XX+3		
3964	032437	201	11	0	00	777765		MOVEI	ZZ+1,ZZ-XX	;Setup index register
3965	032440	201	10	0	00	000010		MOVEI	ZZ,ZZ	;Preload ac with 0,,zz
3966	032441	302	10	0	11	000023		CAIE	ZZ,XX(ZZ+1)	*Test indexing
3967								STOP^		
3968	032442	254	04	0	00	032443		HALT	.+1	;Test failed if program halts here
3969	032443	324	00	0	00	032444		JUMPA	.+1	;To loop change this instruction^
3970										
3971										
3972										
3973						001712	SN=SN+1			
3974						000011		ZZ=ZZ+1		
3975						000026		XX=XX+3		
3976	032444	201	12	0	00	777763		MOVEI	ZZ+1,ZZ-XX	;Setup index register
3977	032445	201	11	0	00	000011		MOVEI	ZZ,ZZ	;Preload ac with 0,,zz
3978	032446	302	11	0	12	000026		CAIE	ZZ,XX(ZZ+1)	*Test indexing
3979								STOP^		
3980	032447	254	04	0	00	032450		HALT	.+1	;Test failed if program halts here
3981	032450	324	00	0	00	032451		JUMPA	.+1	;To loop change this instruction^
3982										
3983										
3984										
3985						001713	SN=SN+1			
3986						000012		ZZ=ZZ+1		
3987						000031		XX=XX+3		
3988	032451	201	13	0	00	777761		MOVEI	ZZ+1,ZZ-XX	;Setup index register
3989	032452	201	12	0	00	000012		MOVEI	ZZ,ZZ	;Preload ac with 0,,zz
3990	032453	302	12	0	13	000031		CAIE	ZZ,XX(ZZ+1)	*Test indexing
3991								STOP^		
3992	032454	254	04	0	00	032455		HALT	.+1	;Test failed if program halts here
3993	032455	324	00	0	00	032456		JUMPA	.+1	;To loop change this instruction^
3994										
3995										
3996										
3997						001714	SN=SN+1			
3998						000013		ZZ=ZZ+1		
3999						000034		XX=XX+3		
4000	032456	201	14	0	00	777757		MOVEI	ZZ+1,ZZ-XX	;Setup index register
4001	032457	201	13	0	00	000013		MOVEI	ZZ,ZZ	;Preload ac with 0,,zz
4002	032460	302	13	0	14	000034		CAIE	ZZ,XX(ZZ+1)	*Test indexing
4003								STOP^		
4004	032461	254	04	0	00	032462		HALT	.+1	;Test failed if program halts here
4005	032462	324	00	0	00	032463		JUMPA	.+1	;To loop change this instruction

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4007 ;*****
4008
4009         001715      SN=SN+1
4010         000014      ZZ=ZZ+1
4011         000037      XX=XX+3
4012 032463 201 15 0 00 777755  MOVEI  ZZ+1,ZZ-XX      ;Setup index register
4013 032464 201 14 0 00 000014  MOVEI  ZZ,ZZ          ;Preload ac with 0,,zz
4014 032465 302 14 0 15 000037  CAIE   ZZ,XX(ZZ+1)      ;*Test indexing
4015                                STOP^
4016 032466 254 04 0 00 032467  HALT   .+1              ;Test failed if program halts here
4017 032467 324 00 0 00 032470  JUMPA  .+1              ;To loop change this instruction^
4018
4019 ;*****
4020
4021         001716      SN=SN+1
4022         000015      ZZ=ZZ+1
4023         000042      XX=XX+3
4024 032470 201 16 0 00 777753  MOVEI  ZZ+1,ZZ-XX      ;Setup index register
4025 032471 201 15 0 00 000015  MOVEI  ZZ,ZZ          ;Preload ac with 0,,zz
4026 032472 302 15 0 16 000042  CAIE   ZZ,XX(ZZ+1)      ;*Test indexing
4027                                STOP^
4028 032473 254 04 0 00 032474  HALT   .+1              ;Test failed if program halts here
4029 032474 324 00 0 00 032475  JUMPA  .+1              ;To loop change this instruction^
4030
4031 ;*****
4032
4033         001717      SN=SN+1
4034         000016      ZZ=ZZ+1
4035         000045      XX=XX+3
4036 032475 201 17 0 00 777751  MOVEI  ZZ+1,ZZ-XX      ;Setup index register
4037 032476 201 16 0 00 000016  MOVEI  ZZ,ZZ          ;Preload ac with 0,,zz
4038 032477 302 16 0 17 000045  CAIE   ZZ,XX(ZZ+1)      ;*Test indexing
4039                                STOP^
4040 032500 254 04 0 00 032501  HALT   .+1              ;Test failed if program halts here
4041 032501 324 00 0 00 032502  JUMPA  .+1              ;To loop change this instruction^
4042
4043 ;*****
4044
4045 PAGE
    
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4046          002000          SN=2000
4047          777777 777777          ZZ=-1
4048          777777 777760          XX=-20
4049
4050          ;This test verifies that index register addressing functions correctly. in
4051          ;This test, the index reg is set-up with movei zz+1,zz-xx, where zz+1 is the
4052          ;Index reg. indexing is tested by loading the ac via movei zz,xx(zz+1),
4053          ;Where xx+c(zz+1)=zz. if the result in the ac equals 0,,zz, this test passes.
4054
4055          C2000: REPEAT ^D15,
4056          <SN=SN+1
4057                  ZZ=ZZ+1
4058                  XX=XX+5
4059                  MOVEI    ZZ+1,ZZ-XX          ;Setup index register
4060                  MOVEI    ZZ,XX(ZZ+1)         ;*Test indexing
4061                  CAIE     ZZ,ZZ               ;Pass if c(ac)=0,,address of ac
4062                  STOP
4063
4064          ;*****
4065          >
4066          SN=SN+1
4067                  ZZ=ZZ+1
4068                  XX=XX+5
4069          032502 201 01 0 00 000013          MOVEI    ZZ+1,ZZ-XX          ;Setup index register
4070          032503 201 00 0 01 777765          MOVEI    ZZ,XX(ZZ+1)         ;*Test indexing
4071          032504 302 00 0 00 000000          CAIE     ZZ,ZZ               ;Pass if c(ac)=0,,address of ac
4072                  STOP^
4073          032505 254 04 0 00 032506          HALT     .+1                ;Test failed if program halts here
4074          032506 324 00 0 00 032507          JUMPA    .+1                ;To loop change this instruction^
4075
4076          ;*****
4077
4078          SN=SN+1
4079          002002
4080          000001
4081          777777 777772
4082          032507 201 02 0 00 000007          MOVEI    ZZ+1,ZZ-XX          ;Setup index register
4083          032510 201 01 0 02 777772          MOVEI    ZZ,XX(ZZ+1)         ;*Test indexing
4084          032511 302 01 0 00 000001          CAIE     ZZ,ZZ               ;Pass if c(ac)=0,,address of ac
4085                  STOP^
4086          032512 254 04 0 00 032513          HALT     .+1                ;Test failed if program halts here
4087          032513 324 00 0 00 032514          JUMPA    .+1                ;To loop change this instruction^
4088
4089          ;*****
4090
4091          SN=SN+1
4092          002003
4093          000002
4094          777777 777777
4095          032514 201 03 0 00 000003          MOVEI    ZZ+1,ZZ-XX          ;Setup index register
4096          032515 201 02 0 03 777777          MOVEI    ZZ,XX(ZZ+1)         ;*Test indexing
4097          032516 302 02 0 00 000002          CAIE     ZZ,ZZ               ;Pass if c(ac)=0,,address of ac
4098                  STOP^
4099          032517 254 04 0 00 032520          HALT     .+1                ;Test failed if program halts here
4100          032520 324 00 0 00 032521          JUMPA    .+1                ;To loop change this instruction^
4101
4102          ;*****
    
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Address	Op	Mod	Reg	Imm	Label	Instruction	Comment
4101				002004		SN=SN+1	
4102				000003		ZZ=ZZ+1	
4103				000004		XX=XX+5	
4104				000004		MOVEI ZZ+1,ZZ-XX	;Setup index register
4105	032521	201	04	0 00	777777	MOVEI ZZ,XX(ZZ+1)	;*Test indexing
4106	032522	201	03	0 04	000004	CAIE ZZ,ZZ	;Pass if c(ac)=0,,address of ac
4107	032523	302	03	0 00	000003	STOP^	
4108						HALT .+1	;Test failed if program halts here
4109	032524	254	04	0 00	032525	JUMPA .+1	;To loop change this instruction^
4110	032525	324	00	0 00	032526		
4111							
4112						*****	
4113							
4114				002005		SN=SN+1	
4115				000004		ZZ=ZZ+1	
4116				000011		XX=XX+5	
4117	032526	201	05	0 00	777773	MOVEI ZZ+1,ZZ-XX	;Setup index register
4118	032527	201	04	0 05	000011	MOVEI ZZ,XX(ZZ+1)	;*Test indexing
4119	032530	302	04	0 00	000004	CAIE ZZ,ZZ	;Pass if c(ac)=0,,address of ac
4120						STOP^	
4121	032531	254	04	0 00	032532	HALT .+1	;Test failed if program halts here
4122	032532	324	00	0 00	032533	JUMPA .+1	;To loop change this instruction^
4123							
4124						*****	
4125							
4126				002006		SN=SN+1	
4127				000005		ZZ=ZZ+1	
4128				000016		XX=XX+5	
4129	032533	201	06	0 00	777767	MOVEI ZZ+1,ZZ-XX	;Setup index register
4130	032534	201	05	0 06	000016	MOVEI ZZ,XX(ZZ+1)	;*Test indexing
4131	032535	302	05	0 00	000005	CAIE ZZ,ZZ	;Pass if c(ac)=0,,address of ac
4132						STOP^	
4133	032536	254	04	0 00	032537	HALT .+1	;Test failed if program halts here
4134	032537	324	00	0 00	032540	JUMPA .+1	;To loop change this instruction^
4135							
4136						*****	
4137							
4138				002007		SN=SN+1	
4139				000006		ZZ=ZZ+1	
4140				000023		XX=XX+5	
4141	032540	201	07	0 00	777763	MOVEI ZZ+1,ZZ-XX	;Setup index register
4142	032541	201	06	0 07	000023	MOVEI ZZ,XX(ZZ+1)	;*Test indexing
4143	032542	302	06	0 00	000006	CAIE ZZ,ZZ	;Pass if c(ac)=0,,address of ac
4144						STOP^	
4145	032543	254	04	0 00	032544	HALT .+1	;Test failed if program halts here
4146	032544	324	00	0 00	032545	JUMPA .+1	;To loop change this instruction^
4147							
4148						*****	
4149							
4150				002010		SN=SN+1	
4151				000007		ZZ=ZZ+1	
4152				000030		XX=XX+5	
4153	032545	201	10	0 00	777757	MOVEI ZZ+1,ZZ-XX	;Setup index register
4154	032546	201	07	0 10	000030	MOVEI ZZ,XX(ZZ+1)	;*Test indexing
4155	032547	302	07	0 00	000007	CAIE ZZ,ZZ	;Pass if c(ac)=0,,address of ac


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4156                                     STOP^
4157 032550 254 04 0 00 032551          HALT      .+1          ;Test failed if program halts here
4158 032551 324 00 0 00 032552          JUMPA     .+1          ;To loop change this instruction^
4159
4160 ;*****
4161
4162                                     SN=SN+1
4163                                     ZZ=ZZ+1
4164                                     XX=XX+5
4165 032552 201 11 0 00 777753          MOVEI     ZZ+1,ZZ-XX      ;Setup index register
4166 032553 201 10 0 11 000035          MOVEI     ZZ,XX(ZZ+1)    ;*Test indexing
4167 032554 302 10 0 00 000010          CAIE      ZZ,ZZ          ;Pass if c(ac)=0,,address of ac
4168                                     STOP^
4169 032555 254 04 0 00 032556          HALT      .+1          ;Test failed if program halts here
4170 032556 324 00 0 00 032557          JUMPA     .+1          ;To loop change this instruction^
4171
4172 ;*****
4173
4174                                     SN=SN+1
4175                                     ZZ=ZZ+1
4176                                     XX=XX+5
4177 032557 201 12 0 00 777747          MOVEI     ZZ+1,ZZ-XX      ;Setup index register
4178 032560 201 11 0 12 000042          MOVEI     ZZ,XX(ZZ+1)    ;*Test indexing
4179 032561 302 11 0 00 000011          CAIE      ZZ,ZZ          ;Pass if c(ac)=0,,address of ac
4180                                     STOP^
4181 032562 254 04 0 00 032563          HALT      .+1          ;Test failed if program halts here
4182 032563 324 00 0 00 032564          JUMPA     .+1          ;To loop change this instruction^
4183
4184 ;*****
4185
4186                                     SN=SN+1
4187                                     ZZ=ZZ+1
4188                                     XX=XX+5
4189 032564 201 13 0 00 777743          MOVEI     ZZ+1,ZZ-XX      ;Setup index register
4190 032565 201 12 0 13 000047          MOVEI     ZZ,XX(ZZ+1)    ;*Test indexing
4191 032566 302 12 0 00 000012          CAIE      ZZ,ZZ          ;Pass if c(ac)=0,,address of ac
4192                                     STOP^
4193 032567 254 04 0 00 032570          HALT      .+1          ;Test failed if program halts here
4194 032570 324 00 0 00 032571          JUMPA     .+1          ;To loop change this instruction^
4195
4196 ;*****
4197
4198                                     SN=SN+1
4199                                     ZZ=ZZ+1
4200                                     XX=XX+5
4201 032571 201 14 0 00 777737          MOVEI     ZZ+1,ZZ-XX      ;Setup index register
4202 032572 201 13 0 14 000054          MOVEI     ZZ,XX(ZZ+1)    ;*Test indexing
4203 032573 302 13 0 00 000013          CAIE      ZZ,ZZ          ;Pass if c(ac)=0,,address of ac
4204                                     STOP^
4205 032574 254 04 0 00 032575          HALT      .+1          ;Test failed if program halts here
4206 032575 324 00 0 00 032576          JUMPA     .+1          ;To loop change this instruction^
4207
4208 ;*****
4209
4210                                     SN=SN+1
4210                                     002015

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4211					000014	ZZ=ZZ+1	
4212					000061	XX=XX+5	
4213	032576	201	15	0	00	777733	MOVEI ZZ+1,ZZ-XX ;Setup index register
4214	032577	201	14	0	15	000061	MOVEI ZZ,XX(ZZ+1) ;*Test indexing
4215	032600	302	14	0	00	000014	CAIE ZZ,ZZ ;Pass if c(ac)=0,,address of ac
4216						STOP^	
4217	032601	254	04	0	00	032602	HALT .+1 ;Test failed if program halts here
4218	032602	324	00	0	00	032603	JUMPA .+1 ;To loop change this instruction^
4219							
4220							*****
4221							SN=SN+1
4222					002016		
4223					000015	ZZ=ZZ+1	
4224					000066	XX=XX+5	
4225	032603	201	16	0	00	777727	MOVEI ZZ+1,ZZ-XX ;Setup index register
4226	032604	201	15	0	16	000066	MOVEI ZZ,XX(ZZ+1) ;*Test indexing
4227	032605	302	15	0	00	000015	CAIE ZZ,ZZ ;Pass if c(ac)=0,,address of ac
4228						STOP^	
4229	032606	254	04	0	00	032607	HALT .+1 ;Test failed if program halts here
4230	032607	324	00	0	00	032610	JUMPA .+1 ;To loop change this instruction^
4231							
4232							*****
4233							SN=SN+1
4234					002017		
4235					000016	ZZ=ZZ+1	
4236					000073	XX=XX+5	
4237	032610	201	17	0	00	777723	MOVEI ZZ+1,ZZ-XX ;Setup index register
4238	032611	201	16	0	17	000073	MOVEI ZZ,XX(ZZ+1) ;*Test indexing
4239	032612	302	16	0	00	000016	CAIE ZZ,ZZ ;Pass if c(ac)=0,,address of ac
4240						STOP^	
4241	032613	254	04	0	00	032614	HALT .+1 ;Test failed if program halts here
4242	032614	324	00	0	00	032615	JUMPA .+1 ;To loop change this instruction^
4243							
4244							*****
4245							

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4246 SUBTTL TEST OF EXCH INSTRUCTION
4247
4248 ;*****
4249
4250 ;This test verifies that exch moves c(e) into ac and moves c(ac) into e.
4251 ;In this case, ac=e=0 and c(ac)=c(e). hence, the final result in ac0
4252 ;Should be 0. if c(ac)=0, the test passes.
4253
4254 032615 400 00 0 00 000000 C2100: SETZ ;Preload ac,e with 0
4255 032616 250 00 0 00 000000 EXCH ;*Exch should place 0 into ac0
4256 032617 332 00 0 00 000000 SKIPE ;Pass if c(ac0)=0
4257 STOP^
4258 032620 254 04 0 00 032621 HALT .+1 ;Test failed if program halts here
4259 032621 324 00 0 00 032622 JUMPA .+1 ;To loop change this instruction^
4260
4261 ;*****
4262
4263 ;This test verifies that exch moves c(e) into ac and moves c(ac) into e.
4264 ;In this case, ac=e=-1,-1 and c(ac)=c(e). hence, the final result in
4265 ;Ac0 should be -1,-1. if c(ac)=-1,-1, the test passes.
4266
4267 032622 474 00 0 00 000000 C2200: SETO ;Preload ac,e with -1,-1
4268 032623 250 00 0 00 000000 EXCH ;*Exch should place -1,-1 into ac0
4269 032624 312 00 0 00 034443 CAME [-1] ;Pass if c(ac0)=-1,-1
4270 STOP^
4271 032625 254 04 0 00 032626 HALT .+1 ;Test failed if program halts here
4272 032626 324 00 0 00 032627 JUMPA .+1 ;To loop change this instruction^
4273
4274 ;*****

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032627 205 00 0 00 777777
032630 201 01 0 00 777777
032631 250 00 0 00 000001
032632 312 01 0 00 034510

032633 254 04 0 00 032634
032634 324 00 0 00 032635
032635 312 00 0 00 034511

032636 254 04 0 00 032637
032637 324 00 0 00 032640

032640 201 00 0 00 777777
032641 205 01 0 00 777777
032642 250 00 0 00 000001
032643 302 01 0 00 777777

032644 254 04 0 00 032645
032645 324 00 0 00 032646
032646 312 00 0 00 034510

032647 254 04 0 00 032650
032650 324 00 0 00 032651

;This test verifies that exch moves c(e) into ac and moves c(ac) into e.
 ;In this case, c(ac)=-1,,0 and c(e)=0,,-1. hence, the final result in
 ;The ac should be 0,,-1 and the result in e should be -1,,0. if these
 ;Results occur, the test passes.

C2400: MOVSI -1 ;Preload ac with -1,,0
 MOVEI 1,-1 ;Preload e with 0,,-1
 EXCH 1 ;*Exch should place 0,,-1 into ac and -1,,0 into e
 CAME 1,[-1,,0] ;Pass if c(e)=-1,,0
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^
 C2410: CAME 0,[0,,-1] ;Pass if c(ac)=0,,-1
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****

;This test verifies that exch moves c(e) into ac and moves c(ac) into e.
 ;In this case, c(ac)=0,,-1 and c(e)=-1,,0. hence, the final result in
 ;The ac should be -1,,0 and the result in e should be 0,,-1. if these
 ;Results occur, the test passes.

C2700: MOVEI -1 ;Preload ac with 0,,-1
 MOVSI 1,-1 ;Preload e with -1,,0
 EXCH 1 ;*Exch should place -1,,0 into ac and 0,,-1 into e
 CAIE 1,-1 ;Pass if c(e)=0,,-1
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^
 C2710: CAME ,[XWD -1,0] ;Pass if c(ac)=-1,,0
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****


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4312 ;This test is a reliability check of exch. first, ac, e are preloaded
4313 ;With 252525,,252525. there, exch is executed 7 times. the ac is then
4314 ;Checked for 252525,,252525. if c(ac)=c(e)=252525,,252525, this test
4315 ;Passes. in this test ac=e=ac0.
4316
4317 032651 200 00 0 00 034512 C3000: MOVE [252525252525] ;Preload ac,e with 252525,,252525
4318 REPEAT 7,
4319 < EXCH ;*Exch should place 252525,,252525 into ac0>
4320 032652 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4321 032653 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4322 032654 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4323 032655 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4324 032656 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4325 032657 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4326 032660 250 00 0 00 000000 EXCH ;*Exch should place 252525,,252525 into ac0
4327 032661 312 00 0 00 034512 CAME [252525252525] ;Pass if c(ac)=252525,,252525
4328 STOP^
4329 032662 254 04 0 00 032663 HALT .+1 ;Test failed if program halts here
4330 032663 324 00 0 00 032664 JUMPA .+1 ;To loop change this instruction^
4331
4332 ;*****
4333
4334 ;This test verifies that exch moves c(ac) into e and c(e) into the ac.
4335 ;In this case, c(ac)=0 and c(e)=-1,,-1. exch is executed 7 times; then,
4336 ;The ac is checked for -1,,-1 and e is checked for 0. if either of these
4337 ;Results are not found, this test fails.
4338
4339 032664 400 00 0 00 000000 C3100: SETZ ;Preload ac with 0
4340 032665 474 01 0 00 000000 SETO 1,0 ;Preload e with -1,,-1
4341 REPEAT 7,
4342 < EXCH 1 ;*Exch should exchange c(ac) and c(e)>
4343 032666 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4344 032667 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4345 032670 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4346 032671 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4347 032672 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4348 032673 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4349 032674 250 00 0 00 000001 EXCH 1 ;*Exch should exchange c(ac) and c(e)
4350 032675 312 00 0 00 034443 CAME [-1] ;Pass if c(ac)=-1,,-1
4351 STOP^
4352 032676 254 04 0 00 032677 HALT .+1 ;Test failed if program halts here
4353 032677 324 00 0 00 032700 JUMPA .+1 ;To loop change this instruction^
4354 032700 312 01 0 00 034513 C3110: CAME 1,[0] ;Pass if c(e)=0
4355 STOP^
4356 032701 254 04 0 00 032702 HALT .+1 ;Test failed if program halts here
4357 032702 324 00 0 00 032703 JUMPA .+1 ;To loop change this instruction^

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032703	474	00	0	00	000000
032704	400	01	0	00	000000
032705	202	00	0	00	000001
032706	312	01	0	00	034443
032707	254	04	0	00	032710
032710	324	00	0	00	032711
032711	312	00	0	00	034443
032712	254	04	0	00	032713
032713	324	00	0	00	032714

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;This test verifies that movem places c(ac) into e and does not modify c(ac)
;In this case, c(ac)=-1,, -1 and c(e)=0. hence, the result in ac and e should
;Be -1,, -1. if c(ac) and c(e)=-1,, -1, this test passes

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C3200:  SETO                ;Preload ac with -1,,-1
        SETZ             1,0 ;Preload e with 0
        MOVEM            1    ;*Movem should place -1,,-1 into e
        CAME             1,[-1] ;Pass if c(e)=-1,,-1
        STOP^
        HALT             .+1   ;Test failed if program halts here
        JUMPA            .+1   ;To loop change this instruction^
C3210:  CAME             0,[-1] ;Pass if c(ac)=-1,,-1
        STOP^
        HALT             .+1   ;Test failed if program halts here
        JUMPA            .+1   ;To loop change this instruction^

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4377 SUBTTL TEST OF JFCL INSTRUCTION AND ARITHMETIC FLAGS
4378
4379 ;*****
4380
4381 ;This test verifies that jfcl 17,.,+1 always returns to the next sequential
4382 ;Instruction. if jfcl skips the next instruction, this test fails.
4383
4384 032714 200 00 0 00 034514 C3300: MOVE [HALT ,+3] ;This instruction should not affect the test
4385 032715 255 17 0 00 032716 JFCL 17,.,+1 ;*Jfcl should return to next sequential instruction
4386 032716 304 00 0 00 000000 CAIA ;Skip halt instruction if jfcl passes
4387 STOP^
4388 032717 254 04 0 00 032720 HALT ,+1 ;Test failed if program halts here
4389 032720 324 00 0 00 032721 JUMPA ,+1 ;To loop change this instruction^
4390
4391 ;*****
4392
4393 ;This test verifies that jfcl 17,.,+1 always clears the cry0 flag. addi is
4394 ;Used to set cry0. then, jfcl 17,.,+1 is executed to clear cry0. jfcl 4,.,+2
4395 ;Is executed to determine whether cry0 was reset by the previous jfcl. this
4396 ;Test fails if jfcl 17,.,+1 did not clear cry0.
4397
4398 032721 200 00 0 00 034443 C3400: MOVE [-1] ;Preload ac with -1,.-1
4399 032722 271 00 0 00 000001 ADDI 1 ;Set cry0 flag
4400 032723 255 17 0 00 032724 JFCL 17,.,+1 ;*Clear arithmetic flags
4401 032724 255 04 0 00 032726 JFCL 4,.,+2 ;Pass if cry0 was reset by previous instruction
4402 032725 334 00 0 00 000000 SKIPA ;Skip halt if cry0 was cleared
4403 STOP^
4404 032726 254 04 0 00 032727 HALT ,+1 ;Test failed if program halts here
4405 032727 324 00 0 00 032730 JUMPA ,+1 ;To loop change this instruction^
4406
4407 ;*****

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4408 ;This test verifies that jfcl 17,.,+1 always clears the cry1 flag.
4409 ;Addi is used to set cry1. then, jfcl 17,.,+1 is executed to clear cry1.
4410 ;Jfcl 4,.,+2 is executed to determine whether cry1 was reset by the previous jfcl.
4411 ;This test fails if jfcl 17,.,+1 did not clear cry1.
4412
4413 032730 200 00 0 00 034443 C3500: MOVE [-1] ;Preload ac with -1,.,-1
4414 032731 271 00 0 00 000001 ADDI 1 ;Set cry1 flag
4415 032732 255 17 0 00 032733 JFCL 17,.,+1 ;*Clear arithmetic flags
4416 032733 255 02 0 00 032735 JFCL 2,.,+2 ;Pass if cry1 was reset by previous instruction
4417 032734 334 00 0 00 000000 SKIPA ;Skip halt if cry1 was cleared
4418 STOP^
4419 032735 254 04 0 00 032736 HALT .+1 ;Test failed if program halts here
4420 032736 324 00 0 00 032737 JUMPA .+1 ;To loop change this instruction^
4421
4422 ;*****
4423
4424 ;This test verifies that jfcl 17,.,+1 always clears the arov flag.
4425 ;Addi is used to set arov. then, jfcl 17,.,+1 is executed to clear arov.
4426 ;Jfcl 4,.,+2 is executed to determine whether arov was reset by the previous jfcl.
4427 ;This test fails if jfcl 17,.,+1 did not clear arov.
4428
4429 032737 205 00 0 00 400000 C3600: MOVSJ 400000 ;Preload ac with -1,.,-1
4430 032740 270 00 0 00 034442 ADD [XWD 400000,0] ;Set arov flag
4431 032741 255 17 0 00 032742 JFCL 17,.,+1 ;*Clear arithmetic flags
4432 032742 255 10 0 00 032744 JFCL 10,.,+2 ;Pass if arov was reset by previous instruction
4433 032743 334 00 0 00 000000 SKIPA ;Skip halt if arov was cleared
4434 STOP^
4435 032744 254 04 0 00 032745 HALT .+1 ;Test failed if program halts here
4436 032745 324 00 0 00 032746 JUMPA .+1 ;To loop change this instruction^
4437
4438 ;*****

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4439 ;This test verifies that jfcl 0, is a no-op.
4440 ;In this test, add is used to set cry0. then jfcl 0, +2 is executed.
4441 ;If jfcl 0, +2 does not skip the next instruction, this test passes.
4442
4443 032746 205 00 0 00 400000 C3700: MOVSI 400000 ;Preload ac with most negative number
4444 032747 270 00 0 00 034443 ADD [-1] ;Set cry0 flag
4445 032750 255 00 0 00 032752 JFCL +2 ;*Jfcl should return to next sequential instruction
4446 032751 334 00 0 00 000000 SKIPA ;Pass if jfcl did not skip
4447 STOP^
4448 032752 254 04 0 00 032753 HALT +1 ;Test failed if program halts here
4449 032753 324 00 0 00 032754 JUMPA +1 ;To loop change this instruction^
4450
4451 ;*****
4452
4453 ;This test verifies that jfcl 0, is a no-op.
4454 ;In this test, add is used to set cry1. then jfcl 0, +2 is executed.
4455 ;If jfcl 0, +2 does not skip the next instruction, this test passes.
4456
4457 032754 205 00 0 00 200000 C4000: MOVSI 200000 ;Preload ac with most negative number
4458 032755 270 00 0 00 034441 ADD [XWD 200000,0] ;Set cry1 flag
4459 032756 255 00 0 00 032760 JFCL +2 ;*Jfcl should return to next sequential instruction
4460 032757 334 00 0 00 000000 SKIPA ;Pass if jfcl did not skip
4461 STOP^
4462 032760 254 04 0 00 032761 HALT +1 ;Test failed if program halts here
4463 032761 324 00 0 00 032762 JUMPA +1 ;To loop change this instruction^
4464
4465 ;*****

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4466 ;This test verifies that addi has the ability to set an arithmetic flag and
4467 ;That 'jfcl 17,.,+2' jumps whenever any arithmetic flag is set. in this test,
4468 ;Addi should set cry0 and cry1. then, jfcl should skip because a flag was set
4469 ;By addi. if this test fails, addi could have failed to set a flag or jfcl
4470 ;Could have failed to jump when a flag was set.
4471
4472 032762 200 00 0 00 034443 C4100: MOVE [-1] ;Preload ac with all ones
4473 032763 271 00 0 00 000001 ADDI 1 ;*Addi should set cry0/1 flags
4474 032764 255 17 0 00 032766 JFCL 17,.,+2 ;*Jfcl should jump because flags are set
4475 STOP^
4476 032765 254 04 0 00 032766 HALT .+1 ;Test failed if program halts here
4477 032766 324 00 0 00 032767 JUMPA .+1 ;To loop change this instruction^
4478
4479 ;*****
4480
4481 ;This test verifies that cai does not clear any arithmetic flags.
4482 ;First, cry0 and cry1 are set by addi; then cai is executed.
4483 ;Jfcl should jump because flags are set. if jfcl does not jump,
4484 ;The flags were cleared by cai. hence, cai failed.
4485
4486 032767 200 00 0 00 034443 C4200: MOVE [-1] ;Preload ac with -1,.-1
4487 032770 271 00 0 00 000001 ADDI 1 ;Set cry0/1 flags
4488 032771 300 17 0 00 000017 CAI 17,17 ;*Cai should not clear flags
4489 032772 255 17 0 00 032774 JFCL 17,.,+2 ;Pass if cai cleared flags
4490 STOP^
4491 032773 254 04 0 00 032774 HALT .+1 ;Test failed if program halts here
4492 032774 324 00 0 00 032775 JUMPA .+1 ;To loop change this instruction^
4493
4494 ;*****

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4495 ;This test verifies that addi has the ability to set an arithmetic flag and
4496 ;That 'jfcl 17,..+2' jumps whenever any arithmetic flag is set. in this test,
4497 ;Addi should set cry0 and cry1. then jfcl should skip because a flag was set
4498 ;By addi. if this test fails, addi could have failed to set a flag or jfcl
4499 ;Could have failed to jump when a flag was set.
4500
4501 032775 200 00 0 00 034443 (4300: MOVE [-1] ;Preload ac with all ones
4502 032776 271 00 0 00 000001 ADDI 1 ;*Addi should set cry1 flags
4503 032777 255 02 0 00 033001 JFCL 2,..+2 ;*Jfcl should jump because cry1 flag is set
4504 STOP^
4505 033000 254 04 0 00 033001 HALT .+1 ;Test failed if program halts here
4506 033001 324 00 0 00 033002 JUMPA .+1 ;To loop change this instruction^
4507
4508 ;*****
4509
4510 ;This test verifies that addi has the ability to set an arithmetic flag and
4511 ;That 'jfcl 17,..+2' jumps whenever any arithmetic flag is set. in this test,
4512 ;Addi should set cry0 and cry1. then, jfcl should skip because a flag was
4513 ;Set by addi. if this test fails, addi could have failed to set a flag or
4514 ;Jfcl could have failed to jump when a flag was set.
4515
4516 033002 200 00 0 00 034443 (4400: MOVE [-1] ;Preload ac with all ones
4517 033003 271 00 0 00 000001 ADDI 1 ;*Addi should set cry0 flag
4518 033004 255 04 0 00 033006 JFCL 4,..+2 ;*Jfcl should jump because cry0 flag is set
4519 STOP^
4520 033005 254 04 0 00 033006 HALT .+1 ;Test failed if program halts here
4521 033006 324 00 0 00 033007 JUMPA .+1 ;To loop change this instruction^
4522
4523 ;*****

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4524 ;This test verifies that addi has the ability to set an arithmetic flag and
4525 ;That 'jfcl 17, +2' jumps whenever any arithmetic flag is set. because a flag
4526 ;Was set by add. if this test fails, addi could have failed to set a flag or
4527 ;Jfcl could have failed to jump when a flag was set.
4528
4529 033007 205 00 0 00 400000 C4500: MOVSJ 400000 ;Preload ac with all ones
4530 033010 270 00 0 00 034442 ADD [XWD 400000,0] ;*Add should set arov flag
4531 033011 255 10 0 00 033013 JFCL 10, +2 ;*Jfcl should jump because arov flag is set
4532 STOP^
4533 033012 254 04 0 00 033013 HALT .+1 ;Test failed if program halts here
4534 033013 324 00 0 00 033014 JUMPA .+1 ;To loop change this instruction^
4535
4536 ;*****
4537
4538 ;This test verifies that jfcl 17, +1 always clears the floating overflow
4539 ;Flag (fov). first jfcl 17, +1 is executed to clear fov. then, jfcl 1, +2
4540 ;Is executed to determine whether fov was cleared. if fov was clear, this
4541 ;Test passes.
4542
4543 033014 255 17 0 00 033015 C4600: JFCL 17, +1 ;*Clear arithmetic flags
4544 033015 255 01 0 00 033017 JFCL 1, +2 ;Pass if fov was cleared
4545 033016 334 00 0 00 000000 SKIP^ ;Skip halt if test passed
4546 STOP^
4547 033017 254 04 0 00 033020 HALT .+1 ;Test failed if program halts here
4548 033020 324 00 0 00 033021 JUMPA .+1 ;To loop change this instruction^
4549
4550 ;*****

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4551 ;This test verifies that jfcl 13, does not reset cry0.
4552 ;First cry0 and cry1 are set by addi; then, jfcl 13, .+2 is executed
4553 ;To clear all arithmetic flags except cry0.
4554 ;This test passes if jfcl 13, .+1 did not reset cry0.
4555
4556 033021 200 00 0 00 034443 C4700: MOVE [-1] ;Reload ac with -1,.-1
4557 033022 271 00 0 00 000001 ADDI 1 ;Set cry0/1
4558 033023 255 13 0 00 033024 JFCL 13, .+1 ;*Jfcl 13, should not reset cry0
4559 033024 255 04 0 00 033026 JFCL 4, .+2 ;Fail if cry 0 was reset
4560 STOP^
4561 033025 254 04 0 00 033026 HALT .+1 ;Test failed if program halts here
4562 033026 324 00 0 00 033027 JUMPA .+1 ;To loop change this instruction^
4563
4564 ;*****
4565
4566 ;This test verifies that jfcl 15, does not reset cry1.
4567 ;First cry0 and cry1 are set by addi; then, jfcl15, .+2 is executed
4568 ;To clear all arithmetic flags except cry1.
4569 ;This test passes if jfcl 15, .+1 did not reset cry1.
4570
4571 033027 200 00 0 00 034443 C5000: MOVE [-1] ;Preload ac with -1,.-1
4572 033030 271 00 0 00 000001 ADDI 1 ;Set cry0/1
4573 033031 255 15 0 00 033032 JFCL 15, .+1 ;*Jfcl15, should not reset cry0
4574 033032 255 02 0 00 033034 JFCL 2, .+2 ;Fail if cry1 was reset
4575 STOP^
4576 033033 254 04 0 00 033034 HALT .+1 ;Test failed if program halts here
4577 033034 324 00 0 00 033035 JUMPA .+1 ;To loop change this instruction^
4578
4579 ;*****

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4580 ;This test verifies that jfcl 17, does not reset arov.
4581 ;First arov is set by add; then, jfcl 17,..+2 is executed
4582 ;To clear all arithmetic flags except arov.
4583 ;This test passes if jfcl 17,..+1 did not reset arov.
4584
4585 033035 205 00 0 00 400000 C5100: MOVSJ 400000 ;Preload ac with -1,..-1
4586 033036 270 00 0 00 034442 ADD [XWD 400000,0] ;Set arov
4587 033037 255 07 0 00 033040 JFCL 7,..+1 ;*Jfcl 17, should not reset arov
4588 033040 255 10 0 00 033042 JFCL 10,..+2 ;Fail if arov was reset
4589 STOP^
4590 033041 254 04 0 00 033042 HALT .+1 ;Test failed if program halts here
4591 033042 324 00 0 00 033043 JUMPA .+1 ;To loop change this instruction^
4592
4593 ;*****
4594
4595 ;This test verifies that add of 0 to 0 will not set arov.
4596 ;First, all flags are reset, then 0 is added to 0 via add.
4597 ;Arov is then checked. if arov is set, this test fails.
4598
4599 033043 255 17 0 00 033044 C5200: JFCL 17,..+1 ;Reset arithmetic flags
4600 033044 400 00 0 00 000000 SETZ ;Preload ac,e with 0
4601 033045 270 00 0 00 000000 ADD ;*Add should not set arov
4602 033046 255 10 0 00 033050 JFCL 10,..+2 ;Pass if arov was reset
4603 033047 334 00 0 00 000000 SKIPA ;Skip halt if add passed
4604 STOP^
4605 033050 254 04 0 00 033051 HALT .+1 ;Test failed if program halts here
4606 033051 324 00 0 00 033052 JUMPA .+1 ;To loop change this instruction^
4607
4608 ;*****

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4609                                     ;This test verifies that add of 0 to 0 will not set cry0.
4610                                     ;First, all flags are reset, then 0 is added to 0 via add.
4611                                     ;Cry0 is then checked.  if cry0 is set, this test fails.
4612
4613
4614 033052 400 00 0 00 000000      C5300: SETZ                ;Reset arithmetic flags
4615 033053 255 17 0 00 033054      JFCL      17,.,+1          ;Preload ac,e with 0
4616 033054 270 00 0 00 000000      ADD                ;*Add should not set cry0
4617 033055 255 04 0 00 033057      JFCL      4,.,+2          ;Pass if cry0 was reset
4618 033056 334 00 0 00 000000      SKIPA             ;Skip halt if add passed
4619                                STOP^
4620 033057 254 04 0 00 033060      HALT      .+1              ;Test failed if program halts here
4621 033060 324 00 0 00 033061      JUMPA     .+1              ;To loop change this instruction^
4622
4623                                     ;*****
4624
4625                                     ;This test verifies that add of 0 to 0 will not set cry1.
4626                                     ;First, all flags are reset, then 0 is added to 0 via add.
4627                                     ;Cry1 is then checked.  if cry1 is set, this test fails.
4628
4629 033061 400 00 0 00 000000      C5400: SETZ                ;Reset arithmetic flags
4630 033062 255 17 0 00 033063      JFCL      17,.,+1          ;Preload ac,e with 0
4631 033063 270 00 0 00 000000      ADD                ;*Add should not set cry1
4632 033064 255 02 0 00 033066      JFCL      2,.,+2          ;Pass if cry1 was reset
4633 033065 334 00 0 00 000000      SKIPA             ;Skip halt if add passed
4634                                STOP^
4635 033066 254 04 0 00 033067      HALT      .+1              ;Test failed if program halts here
4636 033067 324 00 0 00 033070      JUMPA     .+1              ;To loop change this instruction^
4637
4638                                     ;*****

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033070	255	17	0	00	033071
033071	400	00	0	00	000000
033072	300	00	0	00	000000
033073	310	00	0	00	034443
033074	255	17	0	00	033076
033075	334	00	0	00	000000
033076	254	04	0	00	033077
033077	324	00	0	00	033100
033100	255	17	0	00	033101
033101	474	00	0	00	000000
033102	430	00	0	00	034513
033103	430	00	0	00	034443
033104	255	17	0	00	033106
033105	334	00	0	00	000000
033106	254	04	0	00	033107
033107	324	00	0	00	033110

;This test verifies that the 30x and the 31x instruction groups do not affect
;The arithmetic flags. first, the flags are cleared and ac0 is cleared; then,
;Cai and cam are executed. the flags are then checked. if any of the flags
;Are set, this test fails and cai or cam is considered to have erroneously set
;The flags.

C5500:	JFCL	17..+1	;Clear all flags
	SETZ		;Clear ac,0
	CAI		;*Cai should not set any arithmetic flag
	CAM	[-1]	;*Cam should not set any arithmetic flag
	JFCL	17..+2	;Fail if any flag was set
	SKIP		;Skip halt if test passed
	STOP^		
	HALT	.+1	;Test failed if program halts here
	JUMPA	.+1	;To loop change this instruction^

;*****

;This test verifies that the boolean instruction groups do not affect the
;Arithmetic flags. first the flags are cleared and ac0 is cleared; then,
;Xor [0] and xor [-1] are executed. the flags are then checked. if any
;Of the flags are set, this test fails and xor is considered to have
;Erroneously set the flags.

C5600:	JFCL	17..+1	;Clear all flags
	SETO		;Clear ac,0
	XOR	[0]	;*Xor should not set any arithmetic flag
	XOR	[-1]	;*Xor should not set any arithmetic flag
	JFCL	17..+2	;Fail if any flag was set
	SKIP		;Skip halt if test passed
	STOP^		
	HALT	.+1	;Test failed if program halts here
	JUMPA	.+1	;To loop change this instruction^

;*****

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4690033110 474 00 0 00 000000
033111 255 17 0 00 033112
033112 253 00 0 00 033113
033113 252 00 0 00 033114
033114 255 17 0 00 033116
033115 334 00 0 00 000000
033116 254 04 0 00 033117
033117 324 00 0 00 033120

;This test verifies that the aobjx instruction group does do not affect the
;Arithmetic flags. first the flags are cleared and ac0 is cleared; then, aobjn
;And aobjp are executed. the flags are then checked. if any of the flags are
;Set, this test fails and aobjn or aobjp is considered to have erroneously set
;The flags.

C5700: SETO
JFCL 17,+.1
AOBJN .+1
AOBJP .+1
JFCL 17,+.2
SKIPA
STOP^
HALT .+1
JUMPA .+1

;Clear all flags
;Clear ac,0
;*Aobjn should not set any arithmetic arithmetic
;*Aobjp should not set any arithmetic flag
;Fail if any flag was set
;Skip halt if tst passed
;Test failed if program halts here
;To loop change this instruction^

;*****

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 4695 033120 255 17 0 00 033121
 4696 033121 330 00 0 00 034443
 4697 033122 255 17 0 00 033124
 4698 033123 334 00 0 00 000000
 4699
 4700 033124 254 04 0 00 033125
 4701 033125 324 00 0 00 033126
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 4704
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 4706
 4707
 4708
 4709 033126 255 17 0 00 033127
 4710 033127 320 00 0 00 034443
 4711 033130 255 17 0 00 033132
 4712 033131 334 00 0 00 000000
 4713
 4714 033132 254 04 0 00 033133
 4715 033133 324 00 0 00 033134
 4716
 4717

;This test verifies that skip does not affect the flags.
 ;First, the arithmetic flags are cleared; then, skip is executed.
 ;If skip sets arov, cryo, cryl or fov, this test fails.

C5701: JFCL 17,+.1 ;Clear all flags
 SKIP 0,[-1] ;*Skip should not set any flags
 JFCL 17,+.2 ;Fail if any flag is set
 SKIP^ ;Pass if no flag is set
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****

;This test verifies that jump does not affect the flags.
 ;First, the arithmetic flags are cleared; then, jump is executed.
 ;If jump sets arov, cryo, cryl or fov, this test fails.

C5702: JFCL 17,+.1 ;Clear all flags
 JUMP 0,[-1] ;*Jump should not set any flags
 JFCL 17,+.2 ;Fail if any flag is set
 SKIP^ ;Pass if no flag is set
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****

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033134	255	17	0	00	033135
033135	254	00	0	00	033136
033136	255	16	0	00	033140
033137	334	00	0	00	000000
033140	254	04	0	00	033141
033141	324	00	0	00	033142
033142	255	17	0	00	033143
033143	200	02	0	00	000002
033144	255	17	0	00	033146
033145	334	00	0	00	000000
033146	254	04	0	00	033147
033147	324	00	0	00	033150

SUBTTL TEST OF JRST INSTRUCTION AND ARITHMETIC FLAGS

;*****

;This test verifies that 'jrst, 0' does not set any flags.
 ;First the arithmetic flags are reset; then, 'jrst 0, +1' is executed
 ;The arov, cry0 and cry1 flags are then checked. if any
 ;Of these flags are set, this test fails

C6000:	JFCL	17, +1	;Reset all flags
	JRST	+1	;*Jrst should not set any flags
	JFCL	16, +2	;Pass if no flags are set
	SKIPA		;Skip halt if jrst passes
	STOP^		
	HALT	+1	;Test failed if program halts here
	JUMPA	+1	;To loop change this instruction^

;*****

;This test verifies that 'move 2,2' does not set any flags.
 ;First, the arithmetic flags are reset; then, 'move 2,2' is executed.
 ;The fov, arov, cry0 and cry1 flags are then checked. if any
 ;Of these flags are set, this test fails.

C6100:	JFCL	17, +1	;Reset all flags
	MOVE	2, 2	;*Move should not set any flags
	JFCL	17, +2	;Pass if no flags are set
	SKIPA		;Skip halt if move passed
	STOP^		
	HALT	+1	;Test failed if program halts here
	JUMPA	+1	;To loop change this instruction^

;*****

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4751 ;This test verifies that jrst 2,.,+1(1) will set the arithmetic flag
4752 ;Specified in ac1. in this case, ac1 specifies the cry0 flag.
4753 ;First, all flags are reset; then ac1 is set to specify cry0.
4754 ;Next, jrst 2,.,+1(1) is executed to set cry0. cry0 is then checked. if
4755 ;Cry0 is set, this test passes. otherwise, jrst 2,.,+1 is faulty.
4756
4757 033150 255 17 0 00 033151 C6200: JFCL 17,.,+1 ;Clear all flags
4758 SFLAG CRY0 ^;Set cry0 flag
4759
4760 033151 205 01 0 00 200000 MOVSI 1,CRY0
4761 033152 255 17 0 00 033153 JFCL 17,.,+1 ;Reset all flags
4762 033153 254 02 0 01 033154 JRST 2,.,+1(1) ;Set CRY0 flag
4763 033154 255 04 0 00 033156 JFCL 4,.,+2 ;Pass if cry0 is set
4764 STOP^
4765 033155 254 04 0 00 033156 HALT .+1 ;Test failed if program halts here
4766 033156 324 00 0 00 033157 JUMPA .+1 ;To loop change this instruction^
4767
4768 ;*****
4769
4770 ;This test verifies that jrst 2,.,+(1) will set the arithmetic flag
4771 ;Specified in ac1. in this case, ac1 contain 0. hence, jrst 2,.,+1(1)
4772 ;Should reset the arithmetic flags. first, the cry0/1, flags are set by addi;
4773 ;Then the flags should be cleared by jrst 2,.,+1. if cry1 was cleared, the
4774 ;Test passes. otherwise, jrst 2,.,+1 is faulty.
4775
4776 033157 200 00 0 00 034443 C6300: MOVE [-1] ;Preload ac0 with -1,.-1
4777 033160 271 00 0 00 000001 ADDI 1 ;Set cry0/1 flags
4778 SFLAG 0 ^;Reset all arithmetic flags
4779
4780 033161 205 01 0 00 000000 MOVSI 1,0
4781 033162 255 17 0 00 033163 JFCL 17,.,+1 ;Reset all flags
4782 033163 254 02 0 01 033164 JRST 2,.,+1(1) ;Set 0 flag
4783 033164 255 02 0 00 033166 JFCL 2,.,+2 ;Pass if cry1 is reset
4784 033165 334 00 0 00 000000 SKIPA ;Skip halt instruction if test passed
4785 STOP^
4786 033166 254 04 0 00 033167 HALT .+1 ;Test failed if program halts here
4787 033167 324 00 0 00 033170 JUMPA .+1 ;To loop change this instruction^
4788
4789 ;*****

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4790
4791 ;This test verifies that jrst 2,.(1) will set the arithmetic flag
4792 ;Specified in ac1. in this case, ac1 contain 0. hence, jrst 2,.(1)
4793 ;Should reset the arithmetic flags. first, the cry0/1, flags are set by add
4794 ;Then the flags should be cleared by jrst 2,.(1) if arov was cleared, the
4795 ;Test passes. otherwise, jrst 2,.(1) is faulty.
4796
4797 033170 205 00 0 00 400000 C6400: MOVSI 400000 ;Preload ac0 with -1,.-1
4798 033171 270 00 0 00 034443 ADD [-1] ;Set cry0 and arov flags
4799 SFLAG 0 ^;Reset all arithmetic flags
4800
4801 033172 205 01 0 00 000000 MOVSI 1,0
4802 033173 255 17 0 00 033174 JFCL 17,.(1) ;Reset all flags
4803 033174 254 02 0 01 033175 JRST 2,.(1) ;Set 0 flag
4804 033175 255 10 0 00 033177 JFCL 10,.(2) ;Pass if arov is reset
4805 033176 334 00 0 00 000000 SKIPA ;Skip halt instruction if test passed
4806 STOP^
4807 033177 254 04 0 00 033200 HALT .+1 ;Test failed if program halts here
4808 033200 324 00 0 00 033201 JUMPA .+1 ;To loop change this instruction^
4809
4810 ;*****
4811
4812 ;This test verifies that jrst 2,.(1) will set the arithmetic flag
4813 ;Specified in ac1. in this case, ac1 specifies the arov flag.
4814 ;First, all flags are reset; then ac1 set to specify arov.
4815 ;Next, jrst 2,.(1) is executed to set arov. arov is then checked. if
4816 ;Arov is set, this test passes. otherwise, jrst 2,.(1) is faulty.
4817
4818 033201 C6500: SFLAG AROV ^;Set arov flag
4819
4820 033201 205 01 0 00 400000 MOVSI 1,AROV
4821 033202 255 17 0 00 033203 JFCL 17,.(1) ;Reset all flags
4822 033203 254 02 0 01 033204 JRST 2,.(1) ;Set AROV flag
4823 033204 255 10 0 00 033206 JFCL 10,.(2) ;Pass if arov was set
4824 STOP^
4825 033205 254 04 0 00 033206 HALT .+1 ;Test failed if program halts here
4826 033206 324 00 0 00 033207 JUMPA .+1 ;To loop change this instruction^
4827
4828 ;*****

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4829 ;This test verifies that jrst 2,+.1(1) will set the arithmetic flag
4830 ;Specified in ac1. in this case, ac1 specifies the cry1 flag.
4831 ;First, all flags are reset; then ac1 set to specify cry1.
4832 ;Next, jrst 2,+.1(1) is executed to set cry1. cry1 is then checked. if
4833 ;Cry1 is set, this test passes. otherwise, jrst 2,+.1 is faulty.
4834
4835 033207 C6600: SFLAG CRY1 ^;Set cry1 flag
4836
4837 033207 205 01 0 00 100000 MOVSI 1,CRY1
4838 033210 255 17 0 00 033211 JFCL 1,+.1 ;Reset all flags
4839 033211 254 02 0 01 033212 JRST 2,+.1(1) ;Set CRY1 flag
4840 033212 255 02 0 00 033214 JFCL 2,+.2 ;Pass if cry1 was set
4841 STOP^
4842 033213 254 04 0 00 033214 HALT .+1 ;Test failed if program halts here
4843 033214 324 00 0 00 033215 JUMPA .+1 ;To loop change this instruction^
4844
4845 ;*****
4846
4847 ;This test verifies that jrst 2,+.1(1) will set the arithmetic flag
4848 ;Specified in ac1. in this case, ac1 specifies the fov flag.
4849 ;First, all flags are reset; then ac1 set to specify fov.
4850 ;Next, jrst 2,+.1(1) is executed to set fov. fov is then checked. if
4851 ;Fov is set, this test passes. otherwise, jrst 2,+.1 is faulty.
4852
4853 033215 C6700: SFLAG FOV ^;Set fov flag
4854
4855 033215 205 01 0 00 040000 MOVSI 1,FOV
4856 033216 255 17 0 00 033217 JFCL 1,+.1 ;Reset all flags
4857 033217 254 02 0 01 033220 JRST 2,+.1(1) ;Set FOV flag
4858 033220 255 01 0 00 033222 JFCL 1,+.2 ;Pass if fov was set
4859 STOP^
4860 033221 254 04 0 00 033222 HALT .+1 ;Test failed if program halts here
4861 033222 324 00 0 00 033223 JUMPA .+1 ;To loop change this instruction^
4862
4863 ;*****

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4864 ;This test verifies that jfcl 0, should never jump.
4865 ;First, fov is set via jrst2, ;then jfcl 0,
4866 ;Is executed. if jfcl 0, does not skip, this test passes.
4867
4868 033223 C7000: SFLAG FOV ^;Set fov flag
4869
4870 033223 205 01 0 00 040000 MOVSI 1,FOV
4871 033224 255 17 0 00 033225 JFCL 17,..+1 ;Reset all flags
4872 033225 254 02 0 01 033226 JRST 2,..+1(1) ;Set FOV flag
4873 033226 255 00 0 00 033230 JFCL ..+2 ;*Jfcl should not jump
4874 033227 334 00 0 00 000000 SKIPA ;Pass if jfcl did not jump
4875 STOP^
4876 033230 254 04 0 00 033231 HALT .+1 ;Test failed if program halts here
4877 033231 324 00 0 00 033232 JUMPA .+1 ;To loop change this instruction^
4878
4879 ;*****
4880
4881 ;This test verifies that jrst 2,..+1(1) will set the arithmetic flag
4882 ;Specified in ac1. in this case, ac1 contains 0. hence, jrst 2,..+1(1)
4883 ;Should reset the arithmetic flags. first, the cry0, flag is set by
4884 ;Jrst 2,..+1(1) with c(ac1)=cry0. then, the flags should be cleared by
4885 ;Jrst 2,..+1 with c(ac1)=0. if cry0 was cleared, the test passes.
4886 ;Otherwise, jrst 2,..+1 is faulty.
4887
4888 033232 C7100: SFLAG CRY0 ^;Set cry0 flags
4889
4890 033232 205 01 0 00 200000 MOVSI 1,CRY0
4891 033233 255 17 0 00 033234 JFCL 17,..+1 ;Reset all flags
4892 033234 254 02 0 01 033235 JRST 2,..+1(1) ;Set CRY0 flag
4893 033235 400 01 0 00 000000 SETZ 1, ;Setup mask to clear arithmetic flags
4894 033236 255 02 0 01 033237 JRST 2,..+1(1) ;*Reset arithmetic flags
4895 033237 255 04 0 00 033241 JFCL 4,..+2 ;Pass if cry0 flag was reset
4896 033240 334 00 0 00 000000 SKIPA ;Skip halt instruction if test pssed
4897 STOP^
4898 033241 254 04 0 00 033242 HALT .+1 ;Test failed if program halts here
4899 033242 324 00 0 00 033243 JUMPA .+1 ;To loop change this instruction^
4900
4901 ;*****
    
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4902 ;This test verifies that jrst 2,.,+1(1) will set the arithmetic flag
4903 ;Specified in ac1. in this case, ac1 contains 0. hence, jrst 2,.,+1(1)
4904 ;Should reset the arithmetic flags. first, the fov, flag is set by
4905 ;Jrst 2,.,+1(1) with c(ac1)=fov. then, the flags should be cleared by
4906 ;Jrst 2,.,+1 with c(ac1)=0. if fov was cleared, the test passes.
4907 ;Otherwise, jrst 2,.,+1 is faulty.
4908
4909 033243 C7200: SFLAG FOV ^;Set fov flag
4910
4911 033243 205 01 0 00 040000 MOVSI 1,FOV
4912 033244 255 17 0 00 033245 JFCL 17,.,+1 ;Reset all flags
4913 033245 254 02 0 01 033246 JRST 2,.,+1(1) ;Set FOV flag
4914 033246 400 01 0 00 000000 SETZ 1. ;Setup mask to clear arithmetic flags.
4915 033247 254 02 0 01 033250 JRST 2,.,+1(1) ;*Reset arithmetic flags
4916 033250 255 01 0 00 033252 JFCL 1,.,+2 ;Pass if fov flag was reset
4917 033251 334 00 0 00 000000 SKIPA ;Skip halt instruction if test pssed
4918 STOP^
4919 033252 254 04 0 00 033253 HALT .+1 ;Test failed if program halts here
4920 033253 324 00 0 00 033254 JUMPA .+1 ;To loop change this instruction^
4921
4922 ;*****
4923
4924 ;This test verifies that jrst 2,.,+1(1) will set the arithmetic flag
4925 ;Specified in ac1. in this case, ac1 contains 0. hence, jrst 2,.,+1(1)
4926 ;Should reset the arithmetic flags. first, the arithmetic flags are
4927 ;Reset by jfcl 17,.,+1. then, the flags should be cleared by jrst 2,.,+1.
4928 ;If all the arithmetic flags were cleared, the test passes. otherwise,
4929 ;Jrst 2,.,+1 is faulty.
4930
4931 033254 255 17 0 00 033255 C7300: JFCL 17,.,+1 ;Clear flags
4932 033255 400 01 0 00 000000 SETZ 1. ;Setup mask to clear arithmetic flags
4933 033256 254 02 0 01 033257 JRST 2,.,+1(1) ;*Reset arithmetic flags
4934 033257 255 17 0 00 033261 JFCL 17,.,+2 ;Pass if all flags are reset
4935 033260 334 00 0 00 000000 SKIPA ;Skip halt instruction if test passed
4936 STOP^
4937 033261 254 04 0 00 033262 HALT .+1 ;Test failed if program halts here
4938 033262 324 00 0 00 033263 JUMPA .+1 ;To loop change this instruction^
4939
4940 ;*****

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SUBTTL TEST OF JSP INSTRUCTION

;*****

;This test verifies that jsp always stores the flags and pc in the ac.
 ;In this case, the flags are reset; then, jsp is executed. the ac is then
 ;checked for its contents non-zero. if c(ac)=0, it indicates
 ;That neither the flags nor the pc was saved. hence, this test fails.

C7400: SETZB 1 ;Clear ac and setup mask to reset flags
 JRST 2,+.1(1) ;Reset flags
 JSP .+1 ;*Jsp should store flags and pc in the ac
 SKIPN ;Pass if c(ac) is non-zero
 STOP ^;It did not store any flags or pc
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction

;*****

;This test verifies that jsp always stores the pc in the right half of the ac.
 ;In this case, the ac is cleared, then, jsp is executed. the right half of
 ;The ac is then checked for its contents non-zero. if c(ac right half)
 ;Is non-zero, it indicated that the pc was saved; and this test passes.

C7500: SETZ ;Clean ac
 JSP .+1 ;*Jsp should store the pc in the ac
 TRNN -1 ;Pass if c(ac) in non-zero
 STOP^
 HALT .+1 ;Test failed if program halts here
 JUMPA .+1 ;To loop change this instruction^

;*****

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4974 ;This test verifies that jsp always stores the flags in the left half of the ac.
4975 ;First, the ac is cleared; then, some flags are set and jsp is executed.
4976 ;The left half of the ac is checked for its contents non-zero to determine
4977 ;Whether the flags were saved. if c(ac-left) is non-zero, this test passes.
4978
4979 033276 402 00 0 00 000000 C7600: SETZM 0 ;Clear ac
4980 033277 205 01 0 00 740000 MOVSI 1,740000 ;Set up mask to set flags
4981 033300 254 02 0 01 033301 JRST 2,+.1(1) ;Set some arithmetic flags
4982 033301 265 00 0 00 033302 JSP .+1 ;*Jsp should store flags in the ac
4983 033302 607 00 0 00 777777 TLNN -1 ;Pass if c(ac) is non-zero
4984
4985 033303 254 04 0 00 033304 STOP^ ;Test failed if program halts here
4986 033304 324 00 0 00 033305 HALT .+1 ;To loop change this instruction^
4987 JUMPA .+1
4988
4989 ;*****
4990 ;This test verifies that jsp always stores the flags in the left half of the
4991 ;Ac. first, the ac is cleared; then, the arov flag is set and jsp is executed.
4992 ;Then, the arov flag bit of the left half of the ac is checked for its contents
4993 ;Non-zero to determine whether the arov flag was saved. if the arov flag bit
4994 ;Of the ac is set, this test passes.
4995
4996 033305 402 00 0 00 000000 C7700: SETZM 0 ;Clear the ac
4997 SFLAG AROV ^;Set arov flag
4998
4999 033306 205 01 0 00 400000 MOVSI 1,AROV
5000 033307 255 17 0 00 033310 JFCL 17,+.1 ;Reset all flags
5001 033310 254 02 0 01 033311 JRST 2,+.1(1) ;Set AROV flag
5002 033311 265 00 0 00 033312 JSP .+1 ;*Jsp should save the flags in the ac-left
5003 033312 607 00 0 00 400000 TLNN AROV ;Pass if arov was saved
5004 STOP^
5005 033313 254 04 0 00 033314 HALT .+1 ;Test failed if program halts here
5006 033314 324 00 0 00 033315 JUMPA .+1 ;To loop change this instruction^
5007
5008 ;*****

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5009 ;This test verifies that jsp always stores the flags in the left half of the
5010 ;Ac. first, the ac is cleared; then, the cry0 flag is set and jsp is executed.
5011 ;Then, the cry0 flag bit of the left half of the ac is checked for its contents
5012 ;Non-zero to determine whether the cry0 flag was saved. if the cry0 flag bit
5013 ;Of the ac is set, this test passes.
5014
5015 033315 402 00 0 00 000000 C10000: SETZM 0 ;Clear the ac
5016 SFLAG CRY0 ;Set cry0 flag
5017
5018 033316 205 01 0 00 200000 MOVSI 1,CRY0
5019 033317 255 17 0 00 033320 JFCL 17,+.1 ;Reset all flags
5020 033320 254 02 0 01 033321 JRST 2,+.1(1) ;Set CRY0 flag
5021 033321 265 00 0 00 033322 JSP .+1 ;*Jsp should save the flags in the ac-left
5022 033322 607 00 0 00 200000 TLNN CRY0 ;Pass if cry0 was saved
5023 STOP^
5024 033323 254 04 0 00 033324 HALT .+1 ;Test failed if program halts here
5025 033324 324 00 0 00 033325 JUMPA .+1 ;To loop change this instruction^
5026
5027 ;*****
5028
5029 ;This test verifies that jsp always stores the flags in the left half of the
5030 ;Ac. first, the ac is cleared; then, the cry1 flag is set and jsp is executed.
5031 ;Then, the cry1 flag bit of the left half of the ac is checked for its contents
5032 ;Non-zero to determine whether the flag was saved. if the cry1 flag bit of the
5033 ;Ac is set, this test passes.
5034
5035 033325 400 00 0 00 000000 C10100: SETZ ;Clear ac
5036 SFLAG CRY1 ;Set cry1 flag
5037
5038 033326 205 01 0 00 100000 MOVSI 1,CRY1
5039 033327 255 17 0 00 033330 JFCL 17,+.1 ;Reset all flags
5040 033330 254 02 0 01 033331 JRST 2,+.1(1) ;Set CRY1 flag
5041 033331 265 00 0 00 033332 JSP .+1 ;*Jsp should save the flags in the
5042 033332 607 00 0 00 100000 TLNN CRY1 ;Pass if cry1 was saved
5043 STOP^
5044 033333 254 04 0 00 033334 HALT .+1 ;Test failed if program halts here
5045 033334 324 00 0 00 033335 JUMPA .+1 ;To loop change this instruction^
5046
5047 ;*****

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5048 ;This test verifies that jsp always stores the flags in the left half of the
5049 ;Ac. first, the ac is cleared; then, the fov flag is set and jsp is executed.
5050 ;Then, the fov flag bit of the left half of the ac is checked for its contents
5051 ;Non-zero to determine whether the fov flag was saved. if the fov flag bit of
5052 ;The ac is set, this test passes.
5053
5054 033335 400 00 0 00 000000 C10200: SETZ          ;Clear the ac
5055                                SFLAG   FOV          ^;Set fov flag
5056
5057 033336 205 01 0 00 040000      MOVSI   1,FOV
5058 033337 255 17 0 00 033340      JFCL    17,+.1      ;Reset all flags
5059 033340 254 02 0 01 033341      JRST    2,+.1(1)    ;Set FOV flag
5060 033341 265 00 0 00 033342      JSP      .+1        ;*Jsp should save the flags in the ac-left
5061 033342 607 00 0 00 040000      TLNN     FOV          ;Pass if fov was saved
5062                                STOP^
5063 033343 254 04 0 00 033344      HALT     .+1        ;Test failed if program halts here
5064 033344 324 00 0 00 033345      JUMPA    .+1        ;To loop change this instruction^
5065
5066 ;*****
5067
5068 ;This test verifies that jsp will store only flags that exist. i.e. reset
5069 ;Flags will not be set in the ac. only flags that are clearable by jrstrf
5070 ;Will be checked here. first all clearable flags are reset by jrstrf. then
5071 ;Jsp is executed. the ac is then checked. if any clearable flags are set
5072 ;In the ac, this test fails.
5073
5074 033345 C10300: SFLAG   0          ^;Clear all clearable flags
5075
5076 033345 205 01 0 00 000000      MOVSI   1,0
5077 033346 255 17 0 00 033347      JFCL    17,+.1      ;Reset all flags
5078 033347 254 02 0 01 033350      JRST    2,+.1(1)    ;Set 0 flag
5079 033350 265 00 0 00 033351      JSP      .+1        ;*Jsp should not store clearable falgs
5080 033351 603 00 0 00 761777      TLNE     761777      ;Fail if any clearable flag is set
5081                                STOP^
5082 033352 254 04 0 00 033353      HALT     .+1        ;Test failed if program halts here
5083 033353 324 00 0 00 033354      JUMPA    .+1        ;To loop change this instruction^
5084
5085 ;*****
5086
5087 ;This test verifies that jsp always jumps.
5088 ;In this test, jsp .+2 is executed. if jsp jumps, the
5089 ;Test passes. otherwise, this test halts.
5090
5091 033354 265 00 0 00 033356 C10400: JSP      .+2        ;*Jsp should always jump
5092                                STOP^
5093 033355 254 04 0 00 033356      HALT     .+1        ;Test failed if program halts here
5094 033356 324 00 0 00 033357      JUMPA    .+1        ;To loop change this instruction^

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5095          SUBTTL  TEST JRST INSTRUCTION
5096
5097          ;*****
5098
5099          ;This test verifies that jrst always jumps.
5100          ;In this test, jrst .+2 is executed.  if jrst jumps, the test passes;
5101          ;Otherwise, this test halts.
5102
5103 033357 254 00 0 00 033361  C10500: JRST      .+2                ;*Jrst 0, should always jump
5104                                STOP^
5105 033360 254 04 0 00 033361          HALT      .+1                ;Test failed if program halts here
5106 033361 324 00 0 00 033362          JUMPA    .+1                ;To loop change this instruction^
5107
5108          ;*****
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5109          SUBTTL  TEST OF AOBJX INSTRUCTIONS
5110
5111          ;*****
5112
5113          ;This test verifies that aobjn always adds 1 to both halves of the ac.
5114          ;First, the ac is cleared; then, aobjn is executed and the ac is checked
5115          ;For 1,,1.  if c(ac)=1,,1, this test passes.
5116
5117          033362  400 00 0 00 000000      C11200: SETZ          ;Clear the ac
5118          033363  253 00 0 00 033364      AOBJN          .+1          ;*Aobjn should add 1 to both halves of the ac
5119          033364  312 00 0 00 034417      CAME          [XWD 1,1]      ;Pass if c(ac)=1,,1
5120
5121          033365  254 04 0 00 033366      STOP^
5122          033366  324 00 0 00 033367      HALT          .+1          ;Test failed if program halts here
5123
5124
5125          ;*****
5126
5127          ;This test verifies that aobjp always adds 1 to both halves of the ac.
5128          ;First, the ac is cleared; then aobjp is executed and the ac is checked
5129          ;For 1,,1.  if c(ac)=1,,1, this test passes.
5130
5131          033367  200 00 0 00 034515      C11300: MOVE          [XWD 377777,377777] ;Preload ac with 377777,,377777
5132          033370  252 00 0 00 033371      AOBJP          .+1          ;*Aobjp should add 1 to both halves of the ac
5133          033371  312 00 0 00 034516      CAME          [XWD 400000,400000] ;Pass if c(ac)=400000,400000
5134
5135          033372  254 04 0 00 033373      STOP^
5136          033373  324 00 0 00 033374      HALT          .+1          ;Test failed if program halts here
5137
5137          ;*****

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5138 ;This test verifies that aobjn will not jump when c(ac) is positive
5139 ;First, the ac is cleared; and aobjn is executed. aobjn should not jump
5140 ;Because c(ac) is positive. if aobjn jumps, this test fails.
5141
5142 033374 400 00 0 00 000000 C11400: SETZ ;Clear the ac
5143 033375 253 00 0 00 033377 AOBJN .+2 ;*Aobjn should not jump when c(ac) is positive
5144 033376 334 00 0 00 000000 SKIPA ;Pass if aobjn does not jump
5145 STOP^
5146 033377 254 04 0 00 033400 HALT .+1 ;Test failed if program halts here
5147 033400 324 00 0 00 033401 JUMPA .+1 ;To loop change this instruction^
5148
5149 ;*****
5150
5151 ;This test verifies that aobjp will jump when c(ac) is positive
5152 ;First, the ac is cleared; and aobjp is executed. aobjp should jump
5153 ;Because c(ac) is positive. if aobjp does not jump, this test fails.
5154
5155 033401 400 00 0 00 000000 C11500: SETZ ;Clear the ac
5156 033402 252 00 0 00 033404 AOBJP .+2 ;*Aobjp should jump because c(ac) is positive
5157 STOP^
5158 033403 254 04 0 00 033404 HALT .+1 ;Test failed if program halts here
5159 033404 324 00 0 00 033405 JUMPA .+1 ;To loop change this instruction^
5160
5161 ;*****

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5162 ;This test verifies that aobjn will jump when c(ac) is negative. first,
5163 ;The ac is preloaded with 400000,,0; and aobjn is executed. aobjn should
5164 ;Jump because c(ac) is negative. if aobjn does not jump, this test fails.
5165
5166 033405 200 00 0 00 034516 C11600: MOVE [XWD 400000,400000] ;Preload ac with 400000,,400000
5167 033406 253 00 0 00 033410 AOBJN .+2 ;*Aobjn should jump because c(ac) is negative
5168 STOP^
5169 033407 254 04 0 00 033410 HALT .+1 ;Test failed if program halts here
5170 033410 324 00 0 00 033411 JUMPA .+1 ;To loop change this instruction^
5171
5172 ;*****
5173
5174 ;This test verifies that aobjp will not jump when c(ac) is negative. first,
5175 ;The ac is preloaded with 400000,,0; and aobjp is executed. aobjp should not
5176 ;Jump because c(ac) is negative. if aobjp jumps, this test fails.
5177
5178 033411 200 00 0 00 034516 C11700: MOVE [XWD 400000,400000] ;Preload ac with 400000,,400000
5179 033412 252 00 0 00 033414 AOBJP .+2 ;*Aobjp should not jump because c(ac) is negative
5180 033413 334 00 0 00 000000 SKIP^ ;Pass if aobjp does not jump
5181 STOP^
5182 033414 254 04 0 00 033415 HALT .+1 ;Test failed if program halts here
5183 033415 324 00 0 00 033416 JUMPA .+1 ;To loop change this instruction^
5184
5185 ;*****
5186
5187 ;This test verifies that there is no carry from bit 18 to bit 17 of the ac
5188 ;On aobjn. the ac is preloaded with -1,, -1; then aobjn is executed. aobjn
5189 ;Should add one to both halves of the ac without generating a carry from
5190 ;Bit 18 to bit 17. if no carry was generated, this test passes.
5191
5192 033416 474 00 0 00 000000 C12000: SETO ;Preload ac with -1,, -1
5193 033417 253 00 0 00 033420 AOBJN .+1 ;*Aobjn should not cause a carry from bit 18 to 17
5194 033420 332 00 0 00 000000 SKIPE ;Pass if c(ac)=0 (no carry was generated)
5195 STOP^
5196 033421 254 04 0 00 033422 HALT .+1 ;Test failed if program halts here
5197 033422 324 00 0 00 033423 JUMPA .+1 ;To loop change this instruction^
5198
5199 ;*****

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033423	255	17	0	00	033424
033424	211	00	0	00	000000
033425	255	04	0	00	033427
033426	254	04	0	00	033427
033427	324	00	0	00	033430
033430	255	02	0	00	033432
033431	254	04	0	00	033432
033432	324	00	0	00	033433
033433	255	10	0	00	033435
033434	334	00	0	00	000000
033435	254	04	0	00	033436
033436	324	00	0	00	033437
033437	255	01	0	00	033441
033440	334	00	0	00	000000
033441	254	04	0	00	033442
033442	324	00	0	00	033443
033443	255	17	0	00	033444
033444	210	00	0	00	034443
033445	255	17	0	00	033447
033446	334	00	0	00	000000
033447	254	04	0	00	033450
033450	324	00	0	00	033451

SUBTTL TEST SETTING OF ARITHMETIC FLAGS VIA MOVNX AND MOVMX

;This test verifies that movni sets cry0 and cry1 flags only when the data
 ;Is 0. first, the arithmetic flags are reset; then, movni is executed with
 ;Data of zeros. the arithmetic flags are checked. cry0/1 are set and arov
 ;And fov reset, this test passes.

C12100:	JFCL	17,+.1	;Clear flags
	MOVNI	0	;* Movni 0 should set cry0/1
	JCRY0	+.2	;Pass if cry0 is set
	STOP^		
	HALT	+.1	;Test failed if program halts here
	JUMPA	+.1	;To loop change this instruction^
	JCRY1	+.2	;Pass if cry1 is set
	STOP^		
	HALT	+.1	;Test failed if program halts here
	JUMPA	+.1	;To loop change this instruction^
	JOV	+.2	;Pass if arov reset
	SKIPA		
	STOP^		
	HALT	+.1	;Test failed if program halts here
	JUMPA	+.1	;To loop change this instruction^
	JFOV	+.2	;Pass if fov reset
	SKIPA		
	STOP^		
	HALT	+.1	;Test failed if program halts here
	JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that movn will not set arithmetic flags when the data
 ;Is -1,,-1. first, the flags are reset; then, movn [-1,,-1] is executed.
 ;The arithmetic flags are checked. if any arithmetic flag is set, this
 ;Test fails.

C12200:	JFCL	17,+.1	;Clear flags
	MOVN	[-1]	;*Movn [-1,,-1] should set arithmetic flags
	JFCL	17,+.2	;Fail if an arithmetic flag is set
	SKIPA		;Skip halt instruction if movn passed.
	STOP^		
	HALT	+.1	;Test failed if program halts here
	JUMPA	+.1	;To loop change this instruction^

;*****

```

5244      ;This test verifies that movn will set the arov and
5245      ;Cry1 flags only when the data is 400000,0
5246      ;First, the flags are reset; then, movn [400000,,0] is executed.
5247      ;The arithmetic flags are checked.
5248      ;If arov and cry1 are set and cry0 and fov are reset, this test passes.
5249
5250 033451 255 17 0 00 033452      C12300: JFCL      17,+.1      ;Clear arithmetic flags
5251 033452 210 00 0 00 034442      MOVN      [XWD 400000,0]      ;*Movn [400000,,0] should set arov and cry1 only
5252 033453 255 10 0 00 033455      JOV        .+2      ;Pass if arov is set
5253      STOP^
5254 033454 254 04 0 00 033455      HALT        .+1      ;Test failed if program halts here
5255 033455 324 00 0 00 033456      JUMPA       .+1      ;To loop change this instruction^
5256 033456 255 02 0 00 033460      JCRY1       .+2      ;Pass if cry0 is set
5257      STOP^
5258 033457 254 04 0 00 033460      HALT        .+1      ;Test failed if program halts here
5259 033460 324 00 0 00 033461      JUMPA       .+1      ;To loop change this instruction^
5260 033461 255 04 0 00 033463      JCRY0       .+2      ;Pass if cry0 is reset
5261 033462 334 00 0 00 000000      SKIPA
5262      STOP^
5263 033463 254 04 0 00 033464      HALT        .+1      ;Test failed if program halts here
5264 033464 324 00 0 00 033465      JUMPA       .+1      ;To loop change this instruction^
5265 033465 255 01 0 00 033467      JFOV        .+2      ;Pass if fov is reset
5266 033466 334 00 0 00 000000      SKIPA
5267      STOP^
5268 033467 254 04 0 00 033470      HALT        .+1      ;Test failed if program halts here
5269 033470 324 00 0 00 033471      JUMPA       .+1      ;To loop change this instruction^
5270
5271      ;*****

```

```

5272 ;This test verifies that movm will set the arov and
5273 ;cry1 flags only when the data is 400000,0
5274 ;First, the flags are reset; then, movm [400000,,0] is executed.
5275 ;The arithmetic flags are checked.
5276 ;If arov and cry1 are set and cry0 and fov are reset, this test passes.
5277
5278 033471 255 17 0 00 033472 C12301: JFCL 17,+.1 ;Clear arithmetic flags
5279 033472 214 00 0 00 034442 MOVN [XWD 400000,0] ;*Movm [400000,,0] should set arov and cry1 only
5280 033473 255 10 0 00 033475 JOV .+2 ;Pass if arov is set
5281 STOP^
5282 033474 254 04 0 00 033475 HALT .+1 ;Test failed if program halts here
5283 033475 324 00 0 00 033476 JUMPA .+1 ;To loop change this instruction^
5284 033476 255 02 0 00 033500 JCRY1 .+2 ;Pass if cry0 is set
5285 STOP^
5286 033477 254 04 0 00 033500 HALT .+1 ;Test failed if program halts here
5287 033500 324 00 0 00 033501 JUMPA .+1 ;To loop change this instruction^
5288 033501 255 04 0 00 033503 JCRY0 .+2 ;Pass if cry0 is reset
5289 033502 334 00 0 00 000000 SKIPA
5290 STOP^
5291 033503 254 04 0 00 033504 HALT .+1 ;Test failed if program halts here
5292 033504 324 00 0 00 033505 JUMPA .+1 ;To loop change this instruction^
5293 033505 255 01 0 00 033507 JOV .+2 ;Pass if fov is reset
5294 033506 334 00 0 00 000000 SKIPA
5295 STOP^
5296 033507 254 04 0 00 033510 HALT .+1 ;Test failed if program halts here
5297 033510 324 00 0 00 033511 JUMPA .+1 ;To loop change this instruction^
5298
5299 ;*****

```

```

5300 SUBTTL TEST OF AOS AND SOS INSTRUCTIONS
5301
5302 ;*****
5303
5304 ;This test verifies that aos adds 1 to memory and does not skip.
5305 ;First, e is cleared; then, aos is executed. next e is checked for 1.
5306 ;If c(e) is not 1 or aos skipped, this test fails.
5307
5308 033511 400 00 0 00 000000 C12600: SETZ ;Clear e
5309 033512 350 00 0 00 000000 AOS ;*Aos should add 1 to c(e) and not skip
5310 033513 302 00 0 00 000001 CAIE 1 ;Pass if c(e)=0,,1 and aos did not skip
5311 STOP^
5312 033514 254 04 0 00 033515 HALT .+1 ;Test failed if program halts here
5313 033515 324 00 0 00 033516 JUMPA .+1 ;To loop change this instruction^
5314
5315 ;*****
5316
5317 ;This test verifies that aos adds 1 to memory and does not skip. first,
5318 ;E is preloaded with -1,,-1; then, aos is executed. next e is checked for 0.
5319 ;If c(e) is not 0 or aos skipped, this test fails.
5320
5321 033516 474 00 0 00 000000 C12700: SET0 ;Preload e with -1,,-1
5322 033517 350 00 0 00 000000 AOS ;*Aos should add 1 to c(e) and not skip
5323 033520 302 00 0 00 000000 CAIE ;Pass if c(e)=0,,0 and aos did not skip
5324 STOP^
5325 033521 254 04 0 00 033522 HALT .+1 ;Test failed if program halts here
5326 033522 324 00 0 00 033523 JUMPA .+1 ;To loop change this instruction^
5327
5328 ;*****

```



```

5329 ;This test verifies that sos subtracts 1 from memory and does not skip.
5330 ;First, e is cleared; then, sos is executed. next e is checked for -1,,-1.
5331 ;If c(e) is not -1,,-1 or sos skipped, this test fails.
5332
5333 033523 400 00 0 00 000000 C13100: SETZ ;Clear e
5334 033524 370 00 0 00 000000 SOS ;*Sos should subtract 1 from c(e) and not skip
5335 033525 312 00 0 00 034443 CAIE [-1] ;Pass if c(e)=-1,,-1 and sos did not skip
5336 STOP^
5337 033526 254 04 0 00 033527 HALT .+1 ;Test failed if program halts here
5338 033527 324 00 0 00 033530 JUMPA .+1 ;To loop change this instruction^
5339
5340 ;*****
5341
5342 ;This test verifies that sos subtracts 1 from memory and does not skip.
5343 ;First, is preloaded with a; then, sos is executed. next e is checked for 0.
5344 ;If c(e) is not 0 or sos skipped, this test fails.
5345
5346 033530 201 00 0 00 000001 C13200: MOVEI 1 ;Preload e with 1
5347 033531 370 00 0 00 000000 SOS ;*Sos should subtract 1 from c(e) and did not skip
5348 033532 302 00 0 00 000000 CAIE 0 ;Pass if c(e)=0 and sos did not skip
5349 STOP^
5350 033533 254 04 0 00 033534 HALT .+1 ;Test failed if program halts here
5351 033534 324 00 0 00 033535 JUMPA .+1 ;To loop change this instruction^
5352
5353 ;*****
    
```

```

5354 ;This test verifies that sos sets cry0/1 flags if c(e) is a non-zero number
5355 ;Other than 400000,,0. in this case, c(e)=1. first the flags are reset; then
5356 ;Sos is executed. the flags are checked. if cry0 and cry1 are set and arov
5357 ;And fov are reset, this test passes.
5358
5359 033535 255 17 0 00 033536 C13300: JFCL 17,.,+1 ;Reset arithmetic flags
5360 033536 201 00 0 00 000001 MOVEI 1 ;Preload e with 1
5361 033537 370 00 0 00 000000 SOS ;*Sos should set cry0/1
5362 033540 255 04 0 00 033542 JCRY0 .+2 ;Pass if cry0 is set
5363 STOP^
5364 033541 254 04 0 00 033542 HALT .+1 ;Test failed if program halts here
5365 033542 324 00 0 00 033543 JUMPA .+1 ;To loop change this instruction^
5366 033543 255 02 0 00 033545 JCRY1 .+2 ;Pass if cry1 is set
5367 STOP^
5368 033544 254 04 0 00 033545 HALT .+1 ;Test failed if program halts here
5369 033545 324 00 0 00 033546 JUMPA .+1 ;To loop change this instruction^
5370 033546 255 10 0 00 033550 JOV .+2 ;Pass if arov is reset
5371 033547 334 00 0 00 000000 SKIPA
5372 STOP^
5373 033550 254 04 0 00 033551 HALT .+1 ;Test failed if program halts here
5374 033551 324 00 0 00 033552 JUMPA .+1 ;To loop change this instruction^
5375 033552 255 01 0 00 033554 JFOV .+2 ;Pass if fov is reset
5376 033553 334 00 0 00 000000 SKIPA
5377 STOP^
5378 033554 254 04 0 00 033555 HALT .+1 ;Test failed if program halts here
5379 033555 324 00 0 00 033556 JUMPA .+1 ;To loop change this instruction^
5380
5381 ;*****

```

```

5382 ;This test verifies that aos sets cry0 and cry1 flag if c(e) is -1,-1
5383 ;First the flags are reset; then aos is executed. the flags are checked.
5384 ;If cry0 and cry1 are set and arov and fov are reset, this test passes.
5385
5386 033556 255 17 0 00 033557 C13400: JFCL 17,+.1 ;Reset arithmetic flags
5387 033557 474 00 0 00 000000 SETO ;Preload e with 1
5388 033560 350 00 0 00 000000 AOS ;*Aos should set cry0 and cry1
5389 033561 255 04 0 00 033563 JCRY0 .+2 ;Pass if cry0 is set
5390 STOP^
5391 033562 254 04 0 00 033563 HALT .+1 ;Test failed if program halts here
5392 033563 324 00 0 00 033564 JUMPA .+1 ;To loop change this instruction^
5393 033564 255 02 0 00 033566 JCRY1 .+2 ;Pass if cry1 is set
5394 STOP^
5395 033565 254 04 0 00 033566 HALT .+1 ;Test failed if program halts here
5396 033566 324 00 0 00 033567 JUMPA .+1 ;To loop change this instruction^
5397 033567 255 10 0 00 033571 JOV .+2 ;Pass if arov is reset
5398 033570 334 00 0 00 000000 SKIPA
5399 STOP^
5400 033571 254 04 0 00 033572 HALT .+1 ;Test failed if program halts here
5401 033572 324 00 0 00 033573 JUMPA .+1 ;To loop change this instruction^
5402 033573 255 01 0 00 033575 JFOV .+2 ;Pass if fov is reset
5403 033574 334 00 0 00 000000 SKIPA
5404 STOP^
5405 033575 254 04 0 00 033576 HALT .+1 ;Test failed if program halts here
5406 033576 324 00 0 00 033577 JUMPA .+1 ;To loop change this instruction^
5407
5408 ;*****

```

```

5409 SUBTTL TEST OF INTERACTION OF JFCL, JRST, AND JSP WITH ARITHMETIC FLAGS
5410
5411 ;*****
5412
5413 ;This test verifies that jfcl 1, will always clear fov flag.
5414 ;First, fov is set via jrst 2, ;then jfcl 1, .+1 is executed to clear fov.
5415 ;If fov was cleared, this test passes.
5416
5417 033577 C13600: SFLAG FOV ^;Set fov flag
5418
5419 033577 205 01 0 00 040000 MOVSI 1,FOV
5420 033600 255 17 0 00 033601 JFCL 1, .+1 ;Reset all flags
5421 033601 254 02 0 01 033602 JRST 2, .+1(1) ;Set FOV flag
5422 033602 255 01 0 00 033603 JFCL 1, .+1 ;*Jfcl should reset fov
5423 033603 255 01 0 00 033605 JFCL 1, .+2 ;Pass if fov is reset
5424 033604 334 00 0 00 000000 SKIPA ;Skip halt if jfcl 1, .+1 passed
5425 STOP^
5426 033605 254 04 0 00 033606 HALT .+1 ;Test failed if program halts here
5427 033606 324 00 0 00 033607 JUMPA .+1 ;To loop change this instruction^
5428
5429 ;*****
5430
5431 ;This test verifies that jrst 2, can set fxu and jsp can save fxu in the ac.
5432 ;First, fxu is set via jrst 2, ;then, jsp is executed. the ac is checked for
5433 ;Fxu. if fxu is set, this test passes; otherwise, either jrst 2, or jsp failed.
5434
5435 033607 C13700: SFLAG FXU ^;*Set fxu flag
5436
5437 033607 205 01 0 00 000100 MOVSI 1,FXU
5438 033610 255 17 0 00 033611 JFCL 1, .+1 ;Reset all flags
5439 033611 254 02 0 01 033612 JRST 2, .+1(1) ;Set FXU flag
5440 033612 265 00 0 00 033613 JSP .+1 ;*Store fxu flag in ac
5441 033613 607 00 0 00 000100 TLNN FXU ;Pass if fxu is set in the ac
5442 STOP^
5443 033614 254 04 0 00 033615 HALT .+1 ;Test failed if program halts here
5444 033615 324 00 0 00 033616 JUMPA .+1 ;To loop change this instruction^
5445
5446 ;*****

```



```

5447 ;This test verifies that jrst 2, can reset fxu and jsp can save fxu in the ac.
5448 ;First, fxu is set; then, fxu is reset via jrst 2.. next, jsp is executed; and
5449 ;The ac is checked for fxu reset. if fxu is reset in the ac, this test passes;
5450 ;Otherwise, jrst 2, failed to clear fxu or jsp stored fxu incorrectly.
5451
5452 033616 C14000: SFLAG FXU ^;Set fxu flag
5453
5454 033616 205 01 0 00 000100 MOVSI 1,FXU
5455 033617 255 17 0 00 033620 JFCL 17,+.1 ;Reset all flags
5456 033620 254 02 0 01 033621 JRST 2,+.1(1) ;Set FXU flag
5457 SFLAG ^;*Reset fxu flag
5458
5459 033621 205 01 0 00 000000 MOVSI 1,
5460 033622 255 17 0 00 033623 JFCL 17,+.1 ;Reset all flags
5461 033623 254 02 0 01 033624 JRST 2,+.1(1) ;Set flag
5462 033624 265 00 0 00 033625 JSP .+1 ;*Store fxu flag in the ac
5463 033625 603 00 0 00 000100 TLNE FXU ;Pass if fxu is reset in the ac
5464 STOP^
5465 033626 254 04 0 00 033627 HALT .+1 ;Test failed if program halts here
5466 033627 324 00 0 00 033630 JUMPA .+1 ;To loop change this instruction^
5467
5468 ;*****
5469
5470 ;This test verifies that jrst 2, can set dck and jsp can save dck in the ac.
5471 ;First, dck is set via jrst 2, ;then jsp is executed. the ac is checked
5472 ;For dck. if dck is set, this test passes, otherwise jrst 2, or jsp failed.
5473
5474 033630 C14100: SF AG DCK ^;*Set dck flag
5475
5476 033630 205 01 0 00 000040 MOVSI 1,DCK
5477 033631 255 17 0 00 033632 JFCL 17,+.1 ;Reset all flags
5478 033632 254 02 0 01 033633 JRST 2,+.1(1) ;Set DCK flag
5479 033633 265 00 0 00 033634 JSP .+1 ;*Store fxu flag in ac
5480 033634 607 00 0 00 000040 TLNN DCK ;Pass if fxu is set in the ac
5481 STOP^
5482 033635 254 04 0 00 033636 HALT .+1 ;Test failed if program halts here
5483 033636 324 00 0 00 033637 JUMPA .+1 ;To loop change this instruction^
5484
5485 ;*****

```

```

5486      ;This test verifies that jrst 2, can reset dck and jsp can save dck in the ac.
5487      ;First, fxu is set; then, dck is reset via jrst 2.. next, jsp is expected; and
5488      ;The ac is checked for dck reset.  if dck is reset in the ac, this test passes;
5489      ;Otherwise, jrst 2, failed to clear dck or jsp stored dck incorrectly.
5490
5491      033637      C14200: SFLAG      DCK      ^;Set dck flag
5492
5493      033637      205 01 0 00 000040      MOVSI      1,DCK
5494      033640      255 17 0 00 033641      JFCL       17,.,+1      ;Reset all flags
5495      033641      254 02 0 01 033642      JRST       2,.,+1(1)    ;Set DCK flag
5496      ;*Reset dck flag
5497
5498      033642      205 01 0 00 000000      MOVSI      1,
5499      033643      255 17 0 00 033644      JFCL       17,.,+1      ;Reset all flags
5500      033644      254 02 0 01 033645      JRST       2,.,+1(1)    ;Set flag
5501      033645      265 00 0 00 033646      JSP        .+1        ;*Store dck flag in the ac
5502      033646      603 00 0 00 000040      TLNE      DCK        ;Pass if dck is reset in the ac
5503      STOP^
5504      033647      254 04 0 00 033650      HALT        .+1        ;Test failed if program halts here
5505      033650      324 00 0 00 033651      JUMPA      .+1        ;To loop change this instruction^
5506
5507      ;*****

```

```

5508          SUBTTL TEST OF JUMPX INSTRUCTIONS
5509
5510          ;*****
5511
5512          ;This test verifies that jumpl is data dependent. it will jump if and only
5513          ;If c(ac) is negative. in this test, the ac contains -1,-1. hence, jumpl
5514          ;Should jump. if jumpl jumps, this test passes.
5515
5516          033651 474 00 0 00 000000      C14500: SETO                ;Preload ac with -1,-1
5517          033652 321 00 0 00 033654      JUMPL .+2            ;*Jumpl should jump because c(ac) is negative
5518          STOP^
5519          033653 254 04 0 00 033654      HALT .+1              ;Test failed if program halts here
5520          033654 324 00 0 00 033655      JUMPA .+1            ;To loop change this instruction^
5521
5522          ;*****
5523
5524          ;This test verifies that jumpl is data dependent. it will jump if and only
5525          ;If c(ac) is negative. in this test, the ac contains 0. hence, jumpl
5526          ;Should not jump. if jumpl does not jump, this test passes.
5527
5528          033655 400 00 0 00 000000      C14600: SETZ                ;Preload ac with 0
5529          033656 321 00 0 00 033660      JUMPL .+2            ;*Jumpl should not jump
5530          033657 334 00 0 00 000000      SKIPA                ;Pass if jumpl does not jump
5531          STOP^
5532          033660 254 04 0 00 033661      HALT .+1              ;Test failed if program halts here
5533          033661 324 00 0 00 033662      JUMPA .+1            ;To loop change this instruction^
5534
5535          ;*****
5536
5537          ;This test verifies that jumpe is data dependent. it will jump if and
5538          ;Only if c(ac)=0. in this test, the ac contains 0. hence, jumpe should
5539          ;Jump. if jumpe jumps, this test passes.
5540
5541          033662 400 00 0 00 000000      C14700: SETZ                ;Preload ac with 0
5542          033663 322 00 0 00 033665      JUMPE .+2            ;*Jumpe should jump
5543          STOP^
5544          033664 254 04 0 00 033665      HALT .+1              ;Test failed if program halts here
5545          033665 324 00 0 00 033666      JUMPA .+1            ;To loop change this instruction^
5546
5547          ;*****

```

```

5548 ;This test verifies that jumpn is data dependent. it will jump if and
5549 ;Only if c(ac) is non-zero. in this test, the ac contains 1. hence,
5550 ;Jumpn should jump. if jumpn jumps, this test passes.
5551
5552 033666 201 00 0 00 000001 C15000: MOVEI 1 ;Preload ac with 1
5553 033667 326 00 0 00 033671 JUMPN .+2 ;*Jumpn should jump
5554 STOP^
5555 033670 254 04 0 00 033671 HALT .+1 ;Test failed if program halts here
5556 033671 324 00 0 00 033672 JUMPA .+1 ;To loop change this instruction^
5557
5558 ;*****
5559
5560 ;This test verifies that jumpe is data dependent. it will jump if and
5561 ;Only if c(ac)=0. in this test, the ac contains 2. hence, jumpe should
5562 ;Not jump. if jumpe does not jump, this test passes.
5563
5564 033672 201 00 0 00 000002 C15100: MOVEI 2 ;Preload ac with 2
5565 033673 322 00 0 00 033675 JUMPE .+2 ;*Jumpe should not jump
5566 033674 334 00 0 00 000000 SKIPA ;Pass if jumpe did not jump
5567 STOP^
5568 033675 254 04 0 00 033676 HALT .+1 ;Test failed if program halts here
5569 033676 324 00 0 00 033677 JUMPA .+1 ;To loop change this instruction^
5570
5571 ;*****
5572
5573 ;This test verifies that jumpn is data dependent. it will jump if and
5574 ;Only if c(ac) is non-zero. in this test, the ac contains 0. hence,
5575 ;Jumpn should not jump. if jumpn does not jump, this test passes.
5576
5577 033677 400 00 0 00 000000 C15200: SETZ ;Preload ac with 0
5578 033700 320 00 0 00 033702 JUMPN .+2 ;*Jumpn should not jump
5579 033701 334 00 0 00 000000 SKIPA ;Pass if jumpn did not jump
5580 STOP^
5581 033702 254 04 0 00 033703 HALT .+1 ;Test failed if program halts here
5582 033703 324 00 0 00 033704 JUMPA .+1 ;To loop change this instruction^
5583
5584 ;*****

```



```

5585 ;This test verifies that jumpg is data dependent. it will jump if and
5586 ;Only if c(ac) is greater than 0. in this test, the ac contains 1. hence,
5587 ;Jumpg should jump. if jumpg jumps, this test passes.
5588
5589 033704 201 00 0 00 000001 C15300: MOVEI 1 ;Preload ac with 1
5590 033705 327 00 0 00 033707 JUMPG .+2 ;*Jumpg should jump
5591 STOP^
5592 033706 254 04 0 00 033707 HALT .+1 ;Test failed if program halts here
5593 033707 324 00 0 00 033710 JUMPA .+1 ;To loop change this instruction^
5594
5595 ;*****
5596
5597 ;This test verifies that jumpg is data dependent. it will jump if and only
5598 ;If c(ac) is greater than 0. in this test, the ac contains -1,,0. hence,
5599 ;Jumpg should not jump. if jumpg does not jump, this test passes.
5600
5601 033710 205 00 0 00 777777 C15400: MOVSJ -1 ;Preload ac with -1,,0
5602 033711 327 00 0 00 033713 JUMPG .+2 ;*Jumpg should not jump
5603 033712 334 00 0 00 000000 SKIP^ ;Pass if jumpg did not jump
5604 STOP^
5605 033713 254 04 0 00 033714 HALT .+1 ;Test failed if program halts here
5606 033714 324 00 0 00 033715 JUMPA .+1 ;To loop change this instruction^
5607
5608 ;*****
  
```

```

5609 SUBTTL TEST OF AOJ AND SOJ INSTRUCTIONS
5610
5611 ;*****
5612
5613 ;This test verifies that aoj adds 1 to the ac and does not jump.
5614 ;First, the ac is preloaded with 0; then, aoj is executed. next, the
5615 ;Ac is checked for 1. if c(ac) is not 1 or aoj skipped, this test fails.
5616
5617 033715 400 00 0 00 000000 C15500: SETZ ;Preload ac with 0
5618 033716 340 00 0 00 033720 AOJ .+2 ;*Aoj should add 1 to the ac and not jump
5619 033717 302 00 0 00 000001 CAIE 1 ;Pass if c(ac)=1 and aoj did not jump
5620 STOP^
5621 033720 254 04 0 00 033721 HALT .+1 ;Test failed if program halts here
5622 033721 324 00 0 00 033722 JUMPA .+1 ;To loop change this instruction^
5623
5624 ;*****
5625
5626 ;This test verifies that aoj adds 1 to the ac and does not jump.
5627 ;First, the ac is preloaded with -1,, -1; then, aoj is executed. next, the
5628 ;Ac is checked for 0. if c(ac) is not 0 or aoj skipped, this test fails.
5629
5630 033722 474 00 0 00 000000 C15600: SETO ;Preload ac with 0
5631 033723 340 00 0 00 033725 AOJ .+2 ;*Aoj should add 1 to the ac and not jump
5632 033724 302 00 0 00 000000 CAIE 0 ;Pass if c(ac)=1 and aoj did not jump
5633 STOP^
5634 033725 254 04 0 00 033726 HALT .+1 ;Test failed if program halts here
5635 033726 324 00 0 00 033727 JUMPA .+1 ;To loop change this instruction^
5636
5637 ;*****
5638
5639 ;This test verifies that soj subtracts 1 from the ac and does not jump.
5640 ;First, the ac is preloaded with 0; then, soj is executed. next, the ac
5641 ;Is checked for -1,, -1. if c(ac) is not -1,, -1 or soj skipped, this test fails.
5642
5643 033727 400 00 0 00 000000 C15700: SETZ ;Preload ac with 0
5644 033730 360 00 0 00 033732 SOJ .+2 ;*Soj should subtract 1 from the ac and not jump
5645 033731 312 00 0 00 034443 CAME [-1] ;Pass if c(ac)=-1,, -1 and soj did not jump
5646 STOP^
5647 033732 254 04 0 00 033733 HALT .+1 ;Test failed if program halts here
5648 033733 324 00 0 00 033734 JUMPA .+1 ;To loop change this instruction^
5649
5650 ;*****

```

```

5651 ;This test verifies that soj subtracts 1 from the ac and does not jump.
5652 ;First, the ac is preloaded with -1,, -1; then, soj is executed. next, the ac
5653 ;Is checked for -1,, -2. if c(ac) is not -1,, -2 or soj skipped, this test fails.
5654
5655 033734 474 00 0 00 000000 C16000: SETO ;Preload ac with -1,, -1
5656 033735 360 00 0 00 033737 SOJ ;*Soj should subtract 1 from the ac and not jump
5657 033736 312 00 0 00 034444 CAME [-2] ;Pass if c(ac)=-1,, -2 and soj did not jump
5658 STOP^
5659 033737 254 04 0 00 033740 HALT ;Test failed if program halts here
5660 033740 324 00 0 00 033741 JUMPA ;To loop change this instruction^
5661
5662 ;*****
5663
5664 ;This test verifies that soj subtracts 1 from the ac and does not jump.
5665 ;First, the ac is preloaded with 0,, 1; then, soj is executed. next, the
5666 ;Ac is checked for 0. if c(ac) is not 0 or soj skipped, this test fails.
5667
5668 033741 201 00 0 00 000001 C16100: MOVEI 1 ;Preload ac with 1
5669 033742 360 00 0 00 033744 SOJ ;*Soj should subtract 1 from the ac and not jump
5670 033743 302 00 0 00 000000 CAIE 0 ;Pass if c(ac)=0 and soj did not jump
5671 STOP^
5672 033744 254 04 0 00 033745 HALT ;Test failed if program halts here
5673 033745 324 00 0 00 033746 JUMPA ;To loop change this instruction^
5674
5675 ;*****

```

```

5676 ;This test verifies that soj ac, followed by aoj ac, has no net effect on c(ac).
5677 ;In this case, the ac is preloaded with 0; then, soj ac, followed by aoj.
5678 ;Ac, is repeated 7 times. the ac is then checked for its original contents, 0.
5679 ;If c(ac)=0, this test passes; otherwise aoj or soj failed.
5680
5681 000017
5682 033746 400 17 0 00 000000 C16200: AC=17
5683 SETZ AC ;Preload ac with 0
5684 REPEAT ^D10,<
5685 SOJ AC,, ;*Soj should subtract 1 from the ac
5686 AOJ AC,, ;*AoJ should add 1 to the ac>
5687 033747 360 17 0 00 033747 SOJ AC,, ;*Soj should subtract 1 from the ac
5688 033750 340 17 0 00 033750 AOJ AC,, ;*AoJ should add 1 to the ac
5689
5690 033751 360 17 0 00 033751 SOJ AC,, ;*Soj should subtract 1 from the ac
5691 033752 340 17 0 00 033752 AOJ AC,, ;*AoJ should add 1 to the ac
5692
5693 033753 360 17 0 00 033753 SOJ AC,, ;*Soj should subtract 1 from the ac
5694 033754 340 17 0 00 033754 AOJ AC,, ;*AoJ should add 1 to the ac
5695
5696 033755 360 17 0 00 033755 SOJ AC,, ;*Soj should subtract 1 from the ac
5697 033756 340 17 0 00 033756 AOJ AC,, ;*AoJ should add 1 to the ac
5698
5699 033757 360 17 0 00 033757 SOJ AC,, ;*Soj should subtract 1 from the ac
5700 033760 340 17 0 00 033760 AOJ AC,, ;*AoJ should add 1 to the ac
5701
5702 033761 360 17 0 00 033761 SOJ AC,, ;*Soj should subtract 1 from the ac
5703 033762 340 17 0 00 033762 AOJ AC,, ;*AoJ should add 1 to the ac
5704
5705 033763 360 17 0 00 033763 SOJ AC,, ;*Soj should subtract 1 from the ac
5706 033764 340 17 0 00 033764 AOJ AC,, ;*AoJ should add 1 to the ac
5707
5708 033765 360 17 0 00 033765 SOJ AC,, ;*Soj should subtract 1 from the ac
5709 033766 340 17 0 00 033766 AOJ AC,, ;*AoJ should add 1 to the ac
5710
5711 033767 360 17 0 00 033767 SOJ AC,, ;*Soj should subtract 1 from the ac
5712 033770 340 17 0 00 033770 AOJ AC,, ;*AoJ should add 1 to the ac
5713
5714 033771 360 17 0 00 033771 SOJ AC,, ;*Soj should subtract 1 from the ac
5715 033772 340 17 0 00 033772 AOJ AC,, ;*AoJ should add 1 to the ac
5716 033773 332 00 0 00 000017 SKIPE AC ;Pass if c(ac) is unchanged. i.e. c(ac)=0
5717 STOP^
5718 033774 254 04 0 00 033775 HALT .+1 ;Test failed if program halts here
5719 033775 324 00 0 00 033776 JUMPA .+1 ;To loop change this instruction^
5720
5721

```

;*****


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5722 ;This test verifies that soj sets cry0/1 flags if c(e) is a non-zero number
5723 ;Other than 400000,,0. in this case, c(e)=1. first the flags are reset.
5724 ;Then soj is executed. the flags are checked. if cry0 and cry1 are set and
5725 ;Arov and fov are reset, this test passes.
5726
5727 033776 255 17 0 00 033777 C16201: JFCL 17,,+1 ;Reset arithmetic flags
5728 033777 201 00 0 00 000001 MOVEI 1 ;Preload e with 1
5729 034000 360 00 0 00 000000 SOJ ;*Soj should set cry0/1
5730 034001 255 04 0 00 034003 JCRY0 .+2 ;Pass if cry0 is set
5731 STOP^
5732 034002 254 04 0 00 034003 HALT .+1 ;Test failed if program halts here
5733 034003 324 00 0 00 034004 JUMPA .+1 ;To loop change this instruction^
5734 034004 255 02 0 00 034006 JCRY1 .+2 ;Pass if cry1 is set
5735 STOP^
5736 034005 254 04 0 00 034006 HALT .+1 ;Test failed if program halts here
5737 034006 324 00 0 00 034007 JUMPA .+1 ;To loop change this instruction^
5738 034007 255 10 0 00 034011 JOV .+2 ;Pass if arov is reset
5739 034010 334 00 0 00 000000 SKIPA
5740 STOP^
5741 034011 254 04 0 00 034012 HALT .+1 ;Test failed if program halts here
5742 034012 324 00 0 00 034013 JUMPA .+1 ;To loop change this instruction^
5743 034013 255 01 0 00 034015 JFOV .+2 ;Pass if fov is reset
5744 034014 334 00 0 00 000000 SKIPA
5745 STOP^
5746 034015 254 04 0 00 034016 HALT .+1 ;Test failed if program halts here
5747 034016 324 00 0 00 034017 JUMPA .+1 ;To loop change this instruction^
5748
5749 ;*****

```

```

5750 ;This test verifies that aoj sets cry0 and cry1 flag if c(e) is -1,-1.
5751 ;First the flags are reset; then aoj is executed. the flags are checked.
5752 ;If cry0 and cry1 are set and arov and fov are reset, this test passes.
5753
5754 034017 255 17 0 00 034020 C16202: JFCL 17,..+1 ;Reset arithmetic flags
5755 034020 474 00 0 00 000000 SETO ;Preload e with 1
5756 034021 340 00 0 00 000000 AOJ ;*AoJ should set cry0 and cry1
5757 034022 255 04 0 00 034024 JCRY0 .+2 ;Pass if cry0 is set
5758 STOP^
5759 034023 254 04 0 00 034024 HALT .+1 ;Test failed if program halts here
5760 034024 324 00 0 00 034025 JUMPA .+1 ;To loop change this instruction^
5761 034025 255 02 0 00 034027 JCRY1 .+2 ;Pass if cry1 is set
5762 STOP^
5763 034026 254 04 0 00 034027 HALT .+1 ;Test failed if program halts here
5764 034027 324 00 0 00 034030 JUMPA .+1 ;To loop change this instruction^
5765 034030 255 10 0 00 034032 JOV .+2 ;Pass if arov is reset
5766 034031 334 00 0 00 000000 SKIPA
5767 STOP^
5768 034032 254 04 0 00 034033 HALT .+1 ;Test failed if program halts here
5769 034033 324 00 0 00 034034 JUMPA .+1 ;To loop change this instruction^
5770 034034 255 01 0 00 034036 JFOV .+2 ;Pass if fov is reset
5771 034035 334 00 0 00 000000 SKIPA
5772 STOP^
5773 034036 254 04 0 00 034037 HALT .+1 ;Test failed if program halts here
5774 034037 324 00 0 00 034040 JUMPA .+1 ;To loop change this instruction^
5775
5776 ;*****

```

```

5777 SUBTTL TEST OF MEMORY, BOTH AND SELF MODE INSTRUCTIONS
5778
5779 ;*****
5780
5781 ;This test verifies that addm does not modify c(ac)
5782 ;Both ac and e are preloaded with -1,, -1. then addm is executed.
5783 ;This test passes if c(ac) are unchanged.
5784
5785 034040 477 00 0 00 000001 C16400: SETOB 1 ;Preload ac, e with -1,, -1
5786 034041 272 00 0 00 000001 ADDM 1 ;*Addm should not affect c(ac)
5787 034042 312 00 0 00 034443 CAME [-1] ;Pass if c(ac) is unmodified by addm
5788 STOP^
5789 034043 254 04 0 00 034044 HALT .+1 ;Test failed if program halts here
5790 034044 324 00 0 00 034045 JUMPA .+1 ;To loop change this instruction^
5791
5792 ;*****
5793
5794 ;This test verifies that hrrem does not modify c(ac)
5795 ;The ac is preloaded with 0,, -1. then hrrem is executed.
5796 ;This test passes if c(ac) are unchanged.
5797
5798 034045 201 00 0 00 777777 C16500: MOVEI -1 ;Preload ac with 0,, -1
5799 034046 572 00 0 00 000001 HRREM 1 ;*Hrrm should not affect c(ac)
5800 034047 302 00 0 00 777777 CAIE -1 ;Pass if c(ac) is unmodified by hrrem
5801 STOP^
5802 034050 254 04 0 00 034051 HALT .+1 ;Test failed if program halts here
5803 034051 324 00 0 00 034052 JUMPA .+1 ;To loop change this instruction^
5804
5805 ;*****

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```

5806 ;This test verifies that movsm does not modify c(ac).
5807 ;The ac is preloaded with 0,, -1. then movsm is executed.
5808 ;This test passes if c(ac) are unchanged.
5809
5810 034052 201 00 0 00 777777 C16600: MOVEI -1 ;Preload ac with 0,, -1
5811 034053 206 00 0 00 000001 MOVSM 1 ;*Movsm should not affect c(ac)
5812 034054 302 00 0 00 777777 CAIE -1 ;Pass if c(ac) is unmodified by movsm
5813 STOP^
5814 034055 254 04 0 00 034056 HALT .+1 ;Test failed if program halts here
5815 034056 324 00 0 00 034057 JUMPA .+1 ;To loop change this instruction^
5816
5817 ;*****
5818
5819 ;This test verifies that xorm does not modify c(ac).
5820 ;Both ac and e are preloaded with -1,, -1. then xorm is executed.
5821 ;This test passes if c(ac) are unchanged.
5822
5823 034057 477 00 0 00 000001 C16700: SETOB 1 ;Preload ac, e with -1,, -1
5824 034060 432 00 0 00 000001 XORM 1 ;*Xorm should not affect c(ac)
5825 034061 312 00 0 00 034443 CAME [-1] ;Pass if c(ac) is unmodified by xorm
5826 STOP^
5827 034062 254 04 0 00 034063 HALT .+1 ;Test failed if program halts here
5828 034063 324 00 0 00 034064 JUMPA .+1 ;To loop change this instruction^
5829
5830 ;*****

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5831 ;This test verifies that addb adds c(ac) to c(e) and places the result
5832 ;In both ac and e. in this test, both ac and e are preloaded with -1,-1.
5833 ;Then, addb is executed. c(ac) is then compared to c(e) and c(ac) is
5834 ;Compared to -2. if both of these comparisons succeed, this test passes.
5835 ;Otherwise, addb failed.
5836
5837 034064 477 00 0 00 000001 C17000: SETOB 1 ;Preload ac, e with -1,-1
5838 034065 273 00 0 00 000001 ADDB 1 ;*Addb should add c(ac) to c(e) and place result
5839 ;Into both ac and e
5840 034066 312 00 0 00 000001 CAME 1 ;Pass if c(ac)=c(e)
5841 STOP^
5842 034067 254 04 0 00 034070 HALT .+1 ;Test failed if program halts here
5843 034070 324 00 0 00 034071 JUMPA .+1 ;To loop change this instruction^
5844 034071 312 00 0 00 034444 CAME [-2] ;Pass if c(ac)=-2
5845 STOP^
5846 034072 254 04 0 00 034073 HALT .+1 ;Test failed if program halts here
5847 034073 324 00 0 00 034074 JUMPA .+1 ;To loop change this instruction^
5848
5849 ;*****
5850
5851 ;This test verifies that addm adds c(ac) to c(e) and places the result in e
5852 ;In this case, ac, e are both preloaded with -1; then, addm is executed. e is
5853 ;Then checked for -2. if c(e)=-2, this test passes; otherwise, addm failed.
5854
5855 034074 477 00 0 00 000001 C17100: SETOB 1 ;Preload ac, e with -1,-1
5856 034075 272 00 0 00 000001 ADDM 1 ;*Addm should add c(ac) to c(e)
5857 034076 312 01 0 00 034444 CAME 1.[-2] ;Pass if c(e)=-2
5858 STOP^
5859 034077 254 04 0 00 034100 HALT .+1 ;Test failed if program halts here
5860 034100 324 00 0 00 034101 JUMPA .+1 ;To loop change this instruction^
5861
5862 ;*****

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```

5863 ;This test verifies that hllos places ones on the right half of e
5864 ;But does not affect the left half of e. in this case,
5865 ;E is preloaded with 0; the, hllos is executed. the result
5866 ;In e should be 0.,-1. if c(e)=0.,-1, this test passes.
5867
5868 034101 402 00 0 00 000001 C17200: SETZM 1 ;Preload e with 0
5869 034102 523 00 0 00 000001 HLLOS 1 ;*Hllos should place 0.,-1 into e
5870 034103 302 01 0 00 777777 CAIE 1,-1 ;Pass if c(e)=0.,-1
5871 STOP^
5872 034104 254 04 0 00 034105 HALT .+1 ;Test failed if program halts here
5873 034105 324 00 0 00 034106 JUMPA .+1 ;To loop change this instruction^
5874
5875 ;*****
5876
5877 ;This test verifies that movss swaps both halves of e and
5878 ;Places the result in e. in this case, e is preloaded with
5879 ;-1.,0; Then, movss is executed. the result in e should be 0.,-1.
5880 ;If c(e)=0.,-1, this test passes.
5881
5882 034106 205 01 0 00 777777 C17300: MOVSI 1,-1 ;Preload e with -1.,0
5883 034107 207 00 0 00 000001 MOVSS 1 ;*Movss should place 0.,-1 into e
5884 034110 302 01 0 00 777777 CAIE 1,-1 ;Pass if c(e)=0.,-1
5885 STOP^
5886 034111 254 04 0 00 034112 HALT .+1 ;Test failed if program halts here
5887 034112 324 00 0 00 034113 JUMPA .+1 ;To loop change this instruction^
5888
5889 ;*****

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5890      ;This test verifies that aos adds one to memory but does not skip. first,
5891      ;E is preloaded with -1,-1; then, aos is executed. next, e is checked for 0.
5892      ;If c(e) is not 0 or aos skipped, this test fails.
5893
5894      034113  477 00 0 00 000001      C17400: SETOB   1      ;Preload e with -1,-1
5895      034114  350 00 0 00 000001      AOS       1      ;*Aos should add to c(e) and not skip
5896      034115  302 01 0 00 000000      CAIE      1,0     ;Pass if c(e)=0,,0 and aos did not skip
5897      STOP^
5898      034116  254 04 0 00 034117      HALT      .+1     ;Test failed if program halts here
5899      034117  324 00 0 00 034120      JUMPA     .+1     ;To loop change this instruction^
5900
5901      ;*****
5902
5903      ;This test verifies that hrlm places c(ac-right) into e-left and does not
5904      ;Modify e-right. in this case, ac is preloaded with 0 and e is preloaded
5905      ;With -1,-1. then, hrlm is executed. e is then checked for 0,, -1. if
5906      ;C(e)=0,, -1, this test passes.
5907
5908      034120  400 00 0 00 000000      C17500: SETZ    ;Preload ac with 0
5909      034121  474 01 0 00 000000      SETO      1,      ;Preload e with -1,-1
5910      034122  506 00 0 00 000001      HRLM      1      ;*Hrlm should place 0,, -1 into e
5911      034123  302 01 0 00 777777      CAIE      1,-1    ;Pass if c(e)=0,, -1
5912      STOP^
5913      034124  254 04 0 00 034125      HALT      .+1     ;Test failed if program halts here
5914      034125  324 00 0 00 034126      JUMPA     .+1     ;To loop change this instruction^
5915
5916      ;*****

```

```

5917 ;This test verifies that hrrs does not modify e. e is preloaded
5918 ;With 0 and ac is preloaded with -1,-1. hrrs is executed; then
5919 ;E is checked. if c(e) does not change, this test passes.
5920
5921 034126 474 00 0 00 000000 C17600: SET0 ;Preload ac with -1,-1
5922 034127 400 01 0 00 000000 SETZ 1, ;Preload e with 0,0
5923 034130 543 00 0 00 000001 HRRS 1, ;*Hrrs should place 0,0 into e
5924 034131 332 00 0 00 000001 SKIPE 1
5925 STOP^
5926 034132 254 04 0 00 034133 HALT .+1 ;Test failed if program halts here
5927 034133 324 00 0 00 034134 JUMPA .+1 ;To loop change this instruction^
5928
5929 ;*****
5930
5931 ;This test verifies that hrrzm places c(ac-right) into e-right and places
5932 ;Zeros into e-left. in this case, ac=e=ac1 and c(ac)=c(e)=-1,0. hrrzm
5933 ;Is executed and ac1 is checked for 0. if ac1=0, this test passes.
5934
5935 034134 474 00 0 00 000000 C17700: SET0 ;Preload ac0 with -1,-1
5936 034135 205 01 0 00 777777 MOVSI 1,-1 ;Preload ac1 with -1,0
5937 034136 552 01 0 00 000001 HRRZM 1,1 ;*Hrrzm should place 0 into ac1
5938 034137 332 00 0 00 000001 SKIPE 1 ;Pass if c(ac1)=0
5939 STOP^
5940 034140 254 04 0 00 034141 HALT .+1 ;Test failed if program halts here
5941 034141 324 00 0 00 034142 JUMPA .+1 ;To loop change this instruction^
5942
5943 ;*****

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5944      ;This test verifies that jfcl 17,.,+1 never jumps and does not modify c(ac0).
5945      ;First, ac0 is preloaded; then, jfcl is executed.  if ac0 is modified or
5946      ;jfcl skips, this test fails.
5947
5948      034142  400 00 0 00 000000      C20000: SETZ          ;Clear ac0
5949      034143  255 17 0 00 034144      JFCL      17,.,+1      ;*Jfcl should not jump or modify c(ac0).
5950      034144  332 00 0 00 000000      SKIPE          ;Pass if c(ac0)=0 and jfcl did not jump
5951      STOP^
5952      034145  254 04 0 00 034146      HALT      .+1      ;Test failed if program halts here
5953      034146  324 00 0 00 034147      JUMPA     .+1      ;To loop change this instruction^
5954
5955      ;*****
5956
5957      ;This test verifies that xorm performs the logical exclusive or function
5958      ;Between c(ac) and c(e) and places the result into e.  in this case,
5959      ;Ac and e are preloaded with -1,.-1; then, xorm is executed.  if the
5960      ;Result in e is 0, the test passes.
5961
5962      034147  477 00 0 00 000001      C20100: SETOB      1      ;Preload ac,e with -1,.-1
5963      034150  432 00 0 00 000001      XORM       1      ;*Xorm should place 0 into e
5964      034151  302 01 0 00 000000      CAIE      1,0      ;Pass if c(e)=0
5965      STOP^
5966      034152  254 04 0 00 034153      HALT      .+1      ;Test failed if program halts here
5967      034153  324 00 0 00 034154      JUMPA     .+1      ;To loop change this instruction^
5968
5969      ;*****

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```

5970      ;This test verifies that setzb places zeros into both ac and e.
5971      ;After setzb is executed, both ac and e are checked for 0.  if
5972      ;Either ac or e contains any ones, this test fails.
5973
5974      034154  403 00 0 00 000001      C20200: SETZB      1      ;*Setzb should place zeroes in both ac and e
5975      034155  316 00 0 00 034513      CAMN      [0]      ;Fail if c(ac) is non-zero
5976      034156  312 00 0 00 000001      CAME      1      ;Fail if c(e) is non-zero
5977
5978      034157  254 04 0 00 034160      STOP^
5979      034160  324 00 0 00 034161      HALT      .+1      ;Test failed if program halts here
5980      JUMPA      .+1      ;To loop change this instruction^
5981
5982      ;*****
5983      ;This test verifies that setab places c(ac) into both ac and e.
5984      ;First, ac is preloaded with -1,,-1 and e is preloaded with 0;
5985      ;Then, setab is executed.  both ac and e are checked for -1,,-1
5986      ;If either ac or e contain any zeros, this test fails.
5987
5988      034161  400 01 0 00 000000      C20300: SETZ      1,      ;Preload e with 0
5989      034162  474 00 0 00 000000      SETO      ;Preload ac with -1,,-1
5990      034163  427 00 0 00 000001      SETAB      1      ;*Setab should place -1,,-1 into both ac and e
5991      034164  316 00 0 00 034443      CAMN      [-1]      ;Fail if c(ac) is not -1,-1
5992      034165  312 00 0 00 000001      CAME      1      ;Fail if c(e) is not -1,-1
5993
5994      034166  254 04 0 00 034167      STOP^
5995      034167  324 00 0 00 034170      HALT      .+1      ;Test failed if program halts here
5996      JUMPA      .+1      ;To loop change this instruction^
5997
5998      ;*****
  
```

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5998 SUBTTL  XCT INSTRUCTION - BASIC TESTS
5999
6000 ;*****
6001
6002 ;This test verifies that xct will execute the instruction specified by c(e).
6003 ;In this case, c(e) specifies a movei instruction. after executing movei,
6004 ;Control should return to the next sequential instruction following xct. this
6005 ;Test passes if control returns to the next sequential instruction following xct.
6006
6007 034170 403 00 0 00 000001 C20400: SETZB 1 ;Clear ac0 and ac1
6008 034171 256 00 0 00 034517 XCT [MOVEI 1,.,+2] ;*Xct should return control to next instruction
6009 034172 334 00 0 00 000000 SKIPA
6010 STOP^
6011 034173 254 04 0 00 034174 HALT .+1 ;Test failed if program halts here
6012 034174 324 00 0 00 034175 JUMPA .+1 ;To loop change this instruction^
6013
6014 ;*****
6015
6016 ;This test verifies that xct will execute the instruction specified by c(e)
6017 ;In this case, c(e) specifies a movei instruction. after executing movei,
6018 ;The ac specified by movei is checked for 0,,1 (the expected result). if
6019 ;C(ac)=0,,1, this test passes.
6020
6021 034175 403 00 0 00 000001 C20500: SETZB 1 ;Clear ac
6022 034176 256 00 0 00 034520 XCT [MOVEI 1,1] ;*Xct of movei should place 1 in the ac
6023 034177 302 01 0 00 000001 CAIE 1,1 ;Pass if c(ac)=1
6024 STOP^
6025 034200 254 04 0 00 034201 HALT .+1 ;Test failed if program halts here
6026 034201 324 00 0 00 034202 JUMPA .+1 ;To loop change this instruction^
6027
6028 ;*****

```

6029 ;This test verifies that a nest of xct instructions will execute the
 6030 ;Instruction specified by the most nested xct and return control to the
 6031 ;Next sequential instruction following the first xct. in this case, the
 6032 ;Executed instruction is movei. after executing the movei, c(ac) is
 6033 ;Checked for 0,-1 (the expected result). if c(ac)=0,-1, this test passes.
 6034

6035	034202	403	00	0	00	000001	C20600: SETZB	1	;Clear ac
6036	034203	256	00	0	00	034525	XCT	[XCT[XCT[XCT[XCT[MOVEI 1,-1]]]]]	;*Nested xct of movei
6037									;Should place 0,-1 into ac
6038	034204	302	01	0	00	777777	CAIE	1,-1	;Pass if c(ac)=0,-1
6039							STOP^		
6040	034205	254	04	0	00	034206	HALT	+.1	;Test failed if program halts here
6041	034206	324	00	0	00	034207	JUMPA	+.1	;To loop change this instruction^

;*****

6042
 6043 ;This test verifies that xct will not modify an ac which is not specified by
 6044 ;The executed instruction. in this case, ac0 is cleared and then checked for
 6045 ;Zero after the xct instruction is executed. ac0 should not be modified.
 6046
 6047

6048									
6049	034207	403	00	0	00	000001	C20700: SETZB	1	;Clear ac0,ac1
6050	034210	256	00	0	00	034526	XCT	[MOVE 1,[-1]]	;*Xct should not modify ac0
6051	034211	332	00	0	00	000000	SKIPE		;Pass if ac0 was not modified
6052							STOP^		
6053	034212	254	04	0	00	034213	HALT	+.1	;Test failed if program halts here
6054	034213	324	00	0	00	034214	JUMPA	+.1	;To loop change this instruction^

;*****

6055
 6056 ;This test verifies that xct of skipa should return control to
 6057 ;The second sequential instruction following xct.
 6058
 6059

6060									
6061	034214	256	00	0	00	034527	C21000: XCT	[SKIPAJ	;Xct of skipa should return control to .+2
6062							STOP^		
6063	034215	254	04	0	00	034216	HALT	+.1	;Test failed if program halts here
6064	034216	324	00	0	00	034217	JUMPA	+.1	;To loop change this instruction^

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SUBTTL INDIRECT ADDRESSING - BASIC TESTS

;*****

;This test verifies that indirect addressing works when both e and ae
 ;Are within the ac range. the instruction specifying indirect addressing
 ;Is a move. after move is executed, c(ac) is checked for 0, the initial
 ;Contents of the indirect address.

C21100: SETOM	1	;Preload ac with -1,, -1
MOVEI	7,3	;Setup direct address with indirect address
SETZM	3	;Preload indirect address with 0
MOVE	1,a7	;*Fwt from indirect addresss should
		;Place 0 into the ac
SKIPE	1	;Pass if c(ac)=0
STOP^		
HALT	+.1	;Test failed if program halts here
JUMPA	+.1	;To loop change this instruction^

;*****

;This test verifies that indirect addressing works when both e and ae
 ;Are within the ac range. the instruction specifying indirect addressing
 ;Is a move. after move is executed, c(ac) is checked for -1,, -1, the
 ;Initial contents of the indirect address.

C21200: SETZM	1	;Preload ac with -1,, -1
MOVEI	7,3	;Setup direct address with indirect address
SETOM	3	;Preload indirect address with -1,, -1
MOVE	1,a7	;*Fwt from indirect address should
		;Place -1,, -1 into the ac
CAME	1,[-1,, -1]	;Pass if c(ac)=-1,, -1
STOP^		
HALT	+.1	;Test failed if program halts here
JUMPA	+.1	;To loop change this instruction^

;*****

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6102      ;This test verifies that indirect addressing works when both e and ae
6103      ;Are within the ac range. the instruction specifying indirect addressing
6104      ;Is a move. after move is executed, c(ac) is checked for 707070,,707070,
6105      ;The initial contents of the indirect address.
6106
6107      034235 402 00 0 00 000001      C21300: SETZM 1      ;Preload ac with 0
6108      034236 201 07 0 00 000003      MOVEI 7,3      ;Setup direct address with indirect address
6109      034237 200 03 0 00 034530      MOVE 3,[707070,,707070] ;Preload indirect address with 707070,,707070
6110      034240 200 01 1 00 000007      MOVE 1,a7      ;*Fwt from indirect address should
6111      ;Place 707070,,707070 into the ac
6112      034241 312 01 0 00 034530      CAME 1,[707070,,707070] ;Pass if c(ac)=707070,,707070
6113      STOP^
6114      034242 254 04 0 00 034243      HALT .+1      ;Test failed if program halts here
6115      034243 324 00 0 00 034244      JUMPA .+1      ;To loop change this instruction^
6116
6117      ;*****
6118
6119      ;This test verifies that indirect addressing works when e is within the ac
6120      ;Range and ae is beyond the ac range. the instruction specifying indirect
6121      ;Addressing is a move. after move is executed, c(ac) is checked for
6122      ;707070,,707070, The initial contents of the indirect address.
6123
6124      034244 254 00 0 00 034246      C21400: JRST .+2
6125      034245 707070 707070      XWD 707070,707070      ;Indirect address and its data
6126      034246 402 00 0 00 000001      SETZM 1      ;Preload ac with 0
6127      034247 201 07 0 00 034245      MOVEI 7,C21400+1      ;Setup direct address with indirect address
6128      034250 200 01 1 00 000007      MOVE 1,a7      ;*Fwt from indirect address should
6129      ;Place 707070,,707070 into ac
6130      034251 312 01 0 00 034245      CAME 1,C21400+1      ;Pass if c(ac)=707070,,707070
6131      STOP^
6132      034252 254 04 0 00 034253      HALT .+1      ;Test failed if program halts here
6133      034253 324 00 0 00 034254      JUMPA .+1      ;To loop change this instruction^
6134
6135      ;*****
    
```

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6136      ;This test verifies that indirect addressing works when both e and ae
6137      ;Are beyond the ac range. the instruction specifying indirect addressing
6138      ;Is a move. after move is executed, c(ac) is checked for 202020.,202020.
6139      ;The initial contents of the indirect address.
6140
6141 034254 254 00 0 00 034257 C21500: JRST      .+3
6142 034255 000000 034256      .+1
6143 034256 202020 202020      XWD      202020,202020      ;Direct address and its data
6144 034257 402 00 0 00 000001 SETZM      1      ;Indirect address and its data
6145 034260 200 01 1 00 034255 MOVE      1,c21500+1 ;Preload ac with 0
6146      ;*Fwt from indirect address should
6147 034261 312 01 0 00 034256 CAME      1,c21500+2 ;Place 202020.,202020 into ac
6148      ;Pass if c(ac)=202020.,202020
6149 034262 254 04 0 00 034263 HALT      .+1      ;Test failed if program halts here
6150 034263 324 00 0 00 034264 JUMPA     .+1      ;To loop change this instruction^
6151
6152      ;*****
6153
6154      ;This test verifies that indirect addressing works when both e and ae
6155      ;Are beyond the ac range. the instruction specifying indirect
6156      ;Addressing is a came.
6157
6158 034264 254 00 0 00 034267 C21600: JRST      .+3
6159 034265 000000 034266      .+1
6160 034266 272727 272727      XWD      272727,272727      ;Direct address and its data
6161 034267 200 01 0 00 034266 MOVE      1,c21600+2 ;Indirect address and its data
6162 034270 312 01 1 00 034265 CAME      1,c21600+1 ;Preload ac
6163      ;*Came of data from indirect address - non-ac range
6164 034271 254 04 0 00 034272 HALT      .+1      ;Test failed if program halts here
6165 034272 324 00 0 00 034273 JUMPA     .+1      ;To loop change this instruction^
6166
6167      ;*****
6168
6169      ;This test verifies that indirect addressing works when e is within the ac
6170      ;Range and ae is beyond the ac range. the instruction specifying indirect
6171      ;Addressing is a came.
6172
6173 034273 254 00 0 00 034275 C21700: JRST      .+2
6174 034274 252525 252525      XWD      252525,252525      ;Indirect address and its data
6175 034275 201 07 0 00 034274 MOVEI     7,c21700+1 ;Setup direct address with indirect address
6176 034276 200 01 0 00 034274 MOVE      1,c21700+1 ;Setup ac
6177 034277 312 01 1 00 000007 CAME      1,a7      ;*Came if data from indirect address - ac range
6178      ;
6179 034300 254 04 0 00 034301 HALT      .+1      ;Test failed if program halts here
6180 034301 324 00 0 00 034302 JUMPA     .+1      ;To loop change this instruction^

```

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6181 SUBTTL TEST INDIRECT ADDRESSING WITH INDEXING
6182
6183 ;Setup index registers
6184
6185 034302 201 01 0 00 777774 MOVEI 1,-4
6186 034303 201 03 0 00 000002 MOVEI 3,2
6187 034304 201 04 0 00 000010 MOVEI 4,10
6188 034305 201 05 0 00 000001 MOVEI 5,1
6189 034306 201 06 0 00 000005 MOVEI 6,5
6190 034307 201 07 0 00 000007 MOVEI 7,7
6191 034310 201 10 0 00 000004 MOVEI 10,4
6192 034311 201 11 0 00 777772 MOVEI 11,-6
6193 034312 201 12 0 00 000005 MOVEI 12,5
6194 034313 201 13 0 00 000002 MOVEI 13,2
6195
6196 034314 254 00 0 00 034345 JRST C22000 ;Resume test
6197
6198 ;Indirect addressing/indexing test table
6199
6200 :::::::::: :::::::::: ::::::::::
6201
6202 ;Do not modify this table or tests c21700 thru c22600 independently !
6203
6204 :::::::::: :::::::::: ::::::::::
6205
6206 034315 000003 034320 E217: E217A(3)
6207 034316 000020 034323 E220: @E220A
6208 034317 220220 220220 E220B: 220220,,220220
6209 034320 000020 034325 E217A: @E221A ;E221-4
6210 034321 221221 221221 E221B: 221221,,221221
6211 034322 217217 217217 E222A: 217217,,217217 ;E217a+2
6212 034323 000000 034317 E220A: E220B
6213 034324 000000 034324 E221: E221
6214 034325 000000 034321 E221A: E221B
6215 034326 000000 034324 E222: E221
6216 034327 223223 223223 E223A: 223223,,223223
6217 034330 000004 034330 E224A: E224A(4) ;E223-6
6218 034331 222222 222222 E224B: 222222,,222222 ;E222a+7
6219 034332 000000 034332 E225: E225
6220 034333 000007 034322 E222A(7) ;E222+5
6221 034334 000020 034337 @E225A ;E225+2
6222 034335 225225 225225 E225B: 225225,,225225
6223 034336 000000 034336 E223: E223
6224 034337 000000 034335 E225A: E225B
6225 034340 224224 224224 E226B: 224224,,224224 ;E224a+10
6226 034341 226226 226226 E226A: 226226,,226226
6227 034342 000000 034327 E223A: E223A ;E223+4
6228 034343 000025 034343 @E226A(5) ;E223+5
6229 034344 000000 034341 E226B: E226B ;E226a+1
    
```



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6230 ;This test verifies that indirect addressing in combination with indexing
6231 ;Functions correctly. in this case, move 2,@e217 is tested where
6232 ;C(e217)=e217a(3) and c(3)=0,,2. hence, the result in the ac should be
6233 ;C(e217a+2)=217217,,217217 .
6234
6235 034345 476 00 0 00 000002 C22000: SETOM 2 ;Initialize ac
6236 034346 200 02 1 00 034315 MOVE 2,@E217 ;Test indirect addressing with indexing
6237 034347 312 02 0 00 034322 CAME 2,E217A+2 ;Pass if c(ac)=217217,,217217
6238 STOP^
6239 034350 254 04 0 00 034351 HALT .+1 ;Test failed if program halts here
6240 034351 324 00 0 00 034352 JUMPA .+1 ;To loop change this instruction^
6241
6242 ;*****
6243
6244 ;This test verifies that indirect addressing in combination with indexing
6245 ;Functions correctly. in this case, move 2,@e220 is tested where
6246 ;C(e220)=@e220a and c(e220a)=e220b. hence, the result in the ac should
6247 ;Be c(e220b)=220220,,220220 .
6248
6249 034352 402 00 0 00 000002 C22100: SETZM 2 ;Initialize ac
6250 034353 200 02 1 00 034316 MOVE 2,@E220 ;Test indirect addressing with indexing
6251 034354 312 02 0 00 034317 CAME 2,E220B ;Pass if c(ac)=220220,,220220
6252 STOP^
6253 034355 254 04 0 00 034356 HALT .+1 ;Test failed if program halts here
6254 034356 324 00 0 00 034357 JUMPA .+1 ;To loop change this instruction^
6255
6256 ;*****

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6257 ;This test verifies that indirect addressing in combination with indexing
6258 ;Functions correctly. in this case, e221(1) 2, ae217 is tested where c(1)=-4
6259 ;And e221-4=e217a. hence, the result in the ac should be
6260 ;C(e217a)=ae221a=20,,e221a .
6261
6262 034357 476 00 0 00 000002 C22200: SETOM 2 ;Initialize ac
6263 034360 200 02 0 01 034324 MOVE 2,E221(1) ;Test indirect addressing with indexing
6264 034361 312 02 0 00 034320 CAME 2,E217A ;Pass if c(ac)=ae221a=20,,e221a
6265 STOP^
6266 034362 254 04 0 00 034363 HALT .+1 ;Test failed if program halts here
6267 034363 324 00 0 00 034364 JUMPA .+1 ;To loop change this instruction^
6268
6269 ;*****
6270
6271 ;This test verifies that indirect addressing in combination with indexing
6272 ;Functions correctly. in this case, move 2, e222(6) is tested where c(6)=5
6273 ;Hence, the result in the ac should be c(e222+5)=e222a(7)=7,,e222a .
6274
6275 034364 402 00 0 00 000002 C22300: SETZM 2 ;Initialize ac
6276 034365 200 02 0 06 034326 MOVE 2,E222(6) ;Test indirect addressing with indexing
6277 034366 312 02 0 00 034333 CAME 2,E222+5 ;Pass if c(ac)=e222a(7)=7,,e222a
6278 STOP^
6279 034367 254 04 0 00 034370 HALT .+1 ;Test failed if program halts here
6280 034370 324 00 0 00 034371 JUMPA .+1 ;To loop change this instruction^
6281
6282 ;*****

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6283 ;This test verifies that indirect addressing in combination with indexing
6284 ;Functions correctly. in this case, move 2, @e223(10) is tested where c(10)=4
6285 ;And c(e223+4)=e223a. hence, the result in the ac should be
6286 ;c(e223a)=223223,,223223 .
6287
6288 034371 476 00 0 00 000002 C22400: SETOM 2 ;Initialize ac
6289 034372 200 02 1 10 034336 MOVE 2, @E223(10) ;Test indirect addressing with indexing
6290 034373 312 02 0 00 034327 CAME 2, E223A ;Pass if c(ac)=223223,,223223
6291 STOP^
6292 034374 254 04 0 00 034375 HALT .+1 ;Test failed if program halts here
6293 034375 324 00 0 00 034376 JUMPA .+1 ;To loop change this instruction^
6294
6295 ;*****
6296
6297 ;This test verifies that indirect addressing in combination with indexing
6298 ;Functions correctly. in this case, move 2, @e223(11) is tested where
6299 ;c(11)=-6, c(e223-6)=e224a(4) and c(4)=10. hence, the result in the ac
6300 ;Should be c(e224a+10)=224224,,224224 .
6301
6302 034376 402 00 0 00 000002 C22500: SETZM 2 ;Initialize ac
6303 034377 200 02 1 11 034336 MOVE 2, @E223(11) ;Test indirect addressing with indexing
6304 034400 312 02 0 00 034340 CAME 2, E224A+10 ;Pass if c(ac)=224224,,224224
6305 STOP^
6306 034401 254 04 0 00 034402 HALT .+1 ;Test failed if program halts here
6307 034402 324 00 0 00 034403 JUMPA .+1 ;To loop change this instruction^
6308
6309 ;*****

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6310 ;This test verifies that indirect addressing in combination with indexing
6311 ;Functions correctly. in this case, move 2,ae225(13) is tested where c(13)=2,
6312 ;C(e225+2)=ae225a and c(e225a)=e225b. hence, the result in the ac should be
6313 ;C(e225b)=225225,,225225.
6314
6315 034403 476 00 0 00 000002 C22600: SETOM 2 ;Initialize ac
6316 034404 200 02 1 13 034332 MOVE 2,ae225(13) ;Test indirect addressing with indexing
6317 034405 312 02 0 00 034335 CAME 2,E225B ;Pass if c(ac)=225225,,225225
6318 STOP^
6319 034406 254 04 0 00 034407 HALT .+1 ;Test failed if program halts here
6320 034407 324 00 0 00 034410 JUMPA .+1 ;To loop change this instruction^
6321
6322 ;*****
6323
6324 ;This test verifies that indirect addressing in combination with indexing
6325 ;Functions correctly. in this case, move 2,ae223(12) is tested where
6326 ;C(12)=5, c(e223+5)=ae226a(5), c(5)=1 and c(e226a+1)=e226b. hence, the
6327 ;Result in the ac should be c(e226b)=226226,,226226.
6328
6329 034410 402 00 0 00 000002 C22700: SETZM 2 ;Initialize ac
6330 034411 200 02 1 12 034336 MOVE 2,ae223(12) ;Test indirect addressing with indexing
6331 034412 312 02 0 00 034341 CAME 2,E226B ;Pass if c(ac)=226226,,226226
6332 STOP^
6333 034413 254 04 0 00 034414 HALT .+1 ;Test failed if program halts here
6334 034414 324 00 0 00 034415 JUMPA .+1 ;To loop change this instruction^
6335
6336 ;*****
6337
6338
6339 034415 402 00 0 00 034572 ENDIT: SETZM TNUMB#
6340 034416 200 00 0 00 030057 JRST BEGEND

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SUBTTL *STOR* RESERVED STORAGE, SEPT 18,1979

;PROGRAM LITERALS

IFNDEF XLIST
\$LPAPER,<LIST>
LIT

6341			
6342			
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6344			
6345			
6346			
6347	034417		
6348	034417	000001	000001
6349	034420	254 00	0 00 030715
6350	034421	000001	000000
6351	034422	000002	000000
6352	034423	000004	000000
6353	034424	000010	000000
6354	034425	000020	000000
6355	034426	000040	000000
6356	034427	000100	000000
6357	034430	000200	000000
6358	034431	000400	000000
6359	034432	001000	000000
6360	034433	002000	000000
6361	034434	004000	000000
6362	034435	010000	000000
6363	034436	020000	000000
6364	034437	040000	000000
6365	034440	100000	000000
6366	034441	200000	000000
6367	034442	400000	000000
6368	034443	777777	777777
6369	034444	777777	777776
6370	034445	777777	777775
6371	034446	777777	777773
6372	034447	777777	777767
6373	034450	777777	777757
6374	034451	777777	777737
6375	034452	777777	777677
6376	034453	777777	777577
6377	034454	777777	777377
6378	034455	777777	776777
6379	034456	777777	775777
6380	034457	777777	773777
6381	034460	777777	767777
6382	034461	777777	757777
6383	034462	777777	737777
6384	034463	777777	677777
6385	034464	777777	577777
6386	034465	777777	377777
6387	034466	777776	777777
6388	034467	777775	777777
6389	034470	777773	777777
6390	034471	777767	777777
6391	034472	777757	777777
6392	034473	777737	777777
6393	034474	777677	777777
6394	034475	777577	777777
6395	034476	777377	777777

6396	034477	776777	777777
6397	034500	775777	777777
6398	034501	773777	777777
6399	034502	767777	777777
6400	034503	757777	777777
6401	034504	737777	777777
6402	034505	677777	777777
6403	034506	577777	777777
6404	034507	377777	777777
6405	034510	777777	000000
6406	034511	000000	777777
6407	034512	252525	252525
6408	034513	000000	000000
6409	034514	254 04	0 00 032717
6410	034515	377777	377777
6411	034516	400000	400000
6412	034517	201 01	0 00 034173
6413	034520	201 01	0 00 000001
6414	034521	201 01	0 00 777777
6415	034522	256 00	0 00 034521
6416	034523	256 00	0 00 034522
6417	034524	256 00	0 00 034523
6418	034525	256 00	0 00 034524
6419	034526	200 01	0 00 034443
6420	034527	334 00	0 00 000000
6421	034530	707070	707070
6422			
6423	034531	000000	000000
6424			
6425			
6426	034532		
6427			
6428			
6429			
6430	034572		
6431			
6432			
6433	034573	000000	000000
6434			030000

ENDSLD: LIST
0IFDEF DEBUG,<
PATCH: BLOCK DEBUG
>

;PATCHING AREA

;PROGRAM VARIABLES
VARIFDEF PGMEND,<
END: 0
END BEGIN >

NO ERRORS DETECTED

PROGRAM BREAK IS 000000
ABSOLUTE BREAK IS 034574
CPU TIME USED 00:18.819

23P CORE USED

[illegible]

C14600	5528#		
C14700	5541#		
C1500	3007#		
C15000	5552#		
C15100	5564#		
C15200	5577#		
C15300	5589#		
C15400	5601#		
C15500	5617#		
C15600	5630#		
C15700	5643#		
C1600	3426#		
C16000	5655#		
C16100	5668#		
C16200	5681#		
C16201	5727#		
C16202	5754#		
C16400	5785#		
C16500	5798#		
C16600	5810#		
C16700	5823#		
C1700	3854#		
C17000	5837#		
C17100	5855#		
C17200	5868#		
C17300	5882#		
C17400	5894#		
C17500	5908#		
C17600	5921#		
C17700	5935#		
C200	901#		
C2000	4055#		
C20000	5948#		
C20100	5962#		
C20200	5974#		
C20300	5988#		
C20400	6007#		
C20500	6021#		
C20600	6035#		
C20700	6049#		
C2100	4254#		
C21000	6061#		
C21100	6074#		
C21200	6091#		
C21300	6107#		
C21400	6124#	6127	6130
C21500	6141#	6145	6147
C21600	6158#	6161	6162
C21700	6173#	6175	6176
C2200	4267#		
C22000	6196	6235#	
C22100	6249#		
C22200	6262#		

C22300	6275#
C22400	6288#
C22500	6302#
C22600	6315#
C22700	6329#
C2400	4280#
C2410	4287#
C2700	4299#
C2710	4306#
C2720	913#
C3000	4317#
C3100	4339#
C3110	4354#
C3200	4364#
C3210	4371#
C3300	4384#
C3400	4398#
C3500	4413#
C3600	4429#
C3700	4443#
C400	926#
C4000	4457#
C4100	4472#
C4200	4486#
C4300	4501#
C4400	4516#
C4500	4529#
C4600	4543#
C4700	4556#
C500	941#
C5000	4571#
C5100	4585#
C5200	4599#
C5300	4614#
C5400	4629#
C5500	4645#
C5600	4663#
C5700	4680#
C5701	4695#
C5702	4709#
C600	1258#
C6000	4727#
C6100	4742#
C6200	4757#
C6300	4776#
C6400	4797#
C6500	4818#
C6600	4835#
C6700	4853#
C700	1583#
C7000	4868#
C7100	4888#
C7200	4909#

SEQ 0165

C7300	4931#				
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COMMA	554#				
CONSW	429#				
CPOPJ	449#				
CPOPJ1	447#				
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CRY1	360#	4837	5038	5042	
CSHFLG	608#				
CSHMEM	609#				
CTRP	360#				
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DDT	695#				
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DDTSRT	387#				
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DOLLAR	568#				
DONG11	697#	828	841		
DSKUPD	413				
DTE	701#	828	841		
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DTE1	703#				
DTE2	704#				
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E220	6207#	6250			
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E225	6219#	6219	6316					
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IFMMAN	360#							
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SEQ 0167

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MEMSIZ	517#			
MEMTOT	515#			
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MONTYP	640#						
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PAREN8	360#						
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PICHNA	360#						
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PION	360#						
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RTP	564#			
RUNFLG	431#			
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SADR11	53#	397		
SADR2	44#	382		
SADR3	45#	384		
SADR4	46#			
SADR5	47#	445		
SADR6	48#	446		
SADR7	49#	393		
SADR8	50#	394		
SADR9	51#	395		
SBINIT	166	390#		
SCOPE	483#			
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SENSE2	360#			
SENSE3	360#			
SENSE4	360#			
SENSE5	360#			
SENSE6	360#			
SFSTRT	380#			
SLASH	567#			
SM10	671#			
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START2	394#													
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TRPENB	360#													
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TTYFIL	531#													
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SEQ 0174

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USERF	360#	774													
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3549	3565	3565#	3566	3568	3571	3587	3587#	3588	3590	3593	3609	3609#	3610
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3904	3905	3906	3914	3914#	3916	3917	3918	3926	3926#	3928	3929	3930	3938
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\$\$DTE2	793	841#

4

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SEQ 0178

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277 第 277 页
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810
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444

GO HALT

158#	463	746	748	749	753	767	844	891	904	916	929	1003	1019
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1336	1353	1370	1387	1404	1421	1438	1455	1472	1489	1506	1523	1540	1557
1574	1608	1624	1640	1656	1672	1688	1704	1720	1736	1752	1768	1784	1800
1816	1832	1869	1887	1905	1923	1941	1959	1977	1995	2013	2031	2049	2067
2085	2103	2121	2143	2188	2210	2232	2254	2276	2298	2320	2342	2364	2386
2408	2430	2452	2474	2496	2518	2540	2562	2607	2629	2651	2673	2695	2717
2739	2761	2783	2805	2827	2849	2871	2893	2915	2937	2959	2981	2999	3044
3066	3088	3110	3132	3154	3176	3198	3220	3242	3264	3286	3308	3330	3352
3374	3396	3418	3463	3485	3507	3529	3551	3573	3595	3617	3639	3661	3683
3705	3727	3749	3771	3793	3815	3837	3872	3884	3896	3908	3920	3932	3944
3956	3968	3980	3992	4004	4016	4028	4040	4073	4085	4097	4109	4121	4133
4145	4157	4169	4181	4193	4205	4217	4229	4241	4258	4271	4285	4289	4304
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4491	4505	4520	4533	4547	4561	4576	4590	4605	4620	4635	4652	4670	4687
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5169	5182	5196	5211	5215	5220	5225	5240	5254	5258	5263	5268	5282	5286
5291	5296	5312	5325	5337	5350	5364	5368	5373	5378	5391	5395	5400	5405
5426	5443	5465	5482	5504	5519	5532	5544	5555	5568	5581	5592	5605	5621
5634	5647	5659	5672	5718	5732	5736	5741	5746	5759	5763	5768	5773	5789
5802	5814	5827	5842	5846	5859	5872	5886	5898	5913	5926	5940	5952	5966
5978	5994	6011	6025	6040	6053	6063	6081	6098	6114	6132	6149	6164	6179
6239	6253	6266	6279	6292	6306	6319	6333						

JEN
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MAPCNK
MAPMEM
MAPPNT
MAPSET

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PNT3F	213#
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PNT4F	215#
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PNT6F	219#
PNT7	220#
PNT7F	221#
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PNTADR	224#
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PNTCHR	206#
PNTCI	204#
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PNTCW	240#
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PNTDEC	232#
PNTDS	234#
PNTDSF	235#
PNTHW	228#
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SEQ 0180

SEQ 0181

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PNTOCT	226#														
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PNTSIX	237#														
PNTSXF	238#														
PSIXL	198#														
PSIXLF	199#														
PSIXM	202#														
PSIXMF	203#														
PSP	244#														
PSPF	245#														
PUT	155#														
REPTUO	333#														
RTN	154#	450													
S	84#														
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SIXBTZ	261#														
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	1146	1162	1178	1194	1210	1226	1242	1335	1352	1369	1386	1403	1420	1437	
	1454	1471	1488	1505	1522	1539	1556	1573	1607	1623	1639	1655	1671	1687	
	1703	1719	1735	1751	1767	1783	1799	1815	1831	1868	1886	1904	1922	1940	
	1958	1976	1994	2012	2030	2048	2066	2084	2102	2120	2142	2187	2209	2231	
	2253	2275	2297	2319	2341	2363	2385	2407	2429	2451	2473	2495	2517	2539	
	2561	2606	2628	2650	2672	2694	2716	2738	2760	2782	2804	2826	2848	2870	
	2892	2914	2936	2958	2980	2998	3043	3065	3087	3109	3131	3153	3175	3197	
	3219	3241	3263	3285	3307	3329	3351	3373	3395	3417	3462	3484	3506	3528	
	3550	3572	3594	3616	3638	3660	3682	3704	3726	3748	3770	3792	3814	3836	
	3871	3883	3895	3907	3919	3931	3943	3955	3967	3979	3991	4003	4015	4027	
	4039	4072	4084	4096	4108	4120	4132	4144	4156	4168	4180	4192	4204	4216	
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TTYINP

189#
190#

SEQ 0182